Design of a Reusable Rail-to-Rail Operational Amplifier

Pablo Aguirre , Fernando Silveira
Instituto de Ingeniería Eléctrica
Universidad de la República
Montevideo, Uruguay.
paguirre@fing.edu.uy

Abstract

This paper presents a reusable rail-to-rail operational amplifier. The unity-gain bandwidth can be tuned from 7.5kHz to 1.5MHz with total quiescent consumption ranging from $42nA$ to $27.5\mu A$ with 2V supply voltage. A novel rail-to-rail architecture proposed by Duque-Carrillo et al. *and a low-power low-voltage class AB output stage proposed by Silveira* et al. *are integrated to achieve an opamp that meets the requirements of a wide range of applications. A power optimization design methodology for a given settling time is explored and simulations results are presented.*

1. Introduction

Evolution of electronic system design has shown over the last years a strong trend towards the utilization of systems-on-chip (SOC). SOC not only follow the general trend for reducing supply voltage and power but also integrates analog and digital parts. The availability of deep sub-micron technologies on one hand allows the integration of an increasing number of circuits in a single chip making SOC a reality but also make the gap between the complexity of the designs and the designers productivity wider, especially considering the pressures to shrink the products time-to-market. The most accepted solution to bridge this gap in SOC design is the use of reusable functional cells also known as "cores" or "intellectual property" (IP). In the analog design case, the complexity of the problems are much bigger than for their digital counterpart. Not only there are more aspects of the problem to take into account besides consumption, speed and area, but also analog blocks designs are very layout and process dependent and special skills are required to complete them.

One of the most important analog building blocks is the operational amplifier. The need for a reusable opamp cell that meets the demands of several applications is a key objective. To do so it must be capable of operating in different performance and environmental conditions, ie. accept a wide range of input signals and load impedance without significant consumption overheads. Rail-to-rail input stages ([5, 11, 10, 4]) and class AB output stages ([2], [12]) are proposed in the literature to face low power and low supply voltage requirements, maintaining input common mode and dynamic range as well as load driving capabilities. Circuit performance tuning is also a desirable characteristic to enhance the circuit applicability and is being addressed in the academic world ([6, 1]).

In this framework, this work describes the design of a reusable rail-to-rail opamp for low-voltage, low-power applications with performance tuning capabilities. The paper is organized as follows. Section 2 analyzes the architecture of the rail-to-rail input stage. Section 3 presents the complete opamp circuit. In section 4 the design methodology based on a settling time driven power optimization is described. Sections 5 and 6 summarizes the main results and conclusions of this work.

2. Rail-to-rail Input Stage

The ongoing reduction of the power supply voltage in CMOS analog circuits has forced designers to reconsider the usual input stages in operational amplifiers to compensate for the loss of input common mode and dynamic range. The simplest rail-to-rail input stage consists of standard n-channel and p-channel differential pairs driven in parallel [7]. However, this stage is rarely used because its net transconductance gm_T varies by a factor of two over the common mode input range. This variation prevents the design from achieving an optimal frequency compensation, as shown in reference [11]. To obtain a constant gm also has important benefits for the power consumption as shown next. With a varying gm_T, the output stage current has to be greatly increased to keep non-dominant poles far from the worst-case maximum f_T value. Therefore the current saved by having a constant gm makes the extra current spent in

most of constant gm circuits worth it.

Several efforts to obtain a constant gm over the entire common mode input range have been underway for several years now. Initially, the proposed architectures considered only "strong inversion" operation [5, 11] or more recently even only "weak inversion" operation [6, 8]. All these topologies were based on, either, the strong inversion square-law characteristic or the weak inversion exponential one. Although good solutions were achieved in some cases, all of them had a strong dependence in their operation point and can not be used on a programmable opamp that must be able to go from weak to strong inversion without degradation in its performance. This last characteristic allows the opamp cell to be used from low frequency very low power applications to MHz frequency low power applications.

An architecture capable of providing constant gm in all regions of inversion of the MOS transistor appears to be a need in reusable opamp cells. Several topologies have been reported recently [10, 9, 4]. These architectures are usually referred as "universal". Another desirable characteristic is that of being "robust" as defined by Duque-Carrillo *et al.* [4], meaning that the accuracy of the circuit does not rely on any condition for matching n- and p-channel input transistors, i.e. on scaling the geometries to compensate for the difference in mobility between electrons and holes. This allows the circuit not only to be independent of process variations, which are hard to anticipate for the designer, but also to be easily migrated to another technology. The proposed architecture by Duque-Carrillo *et al.* [4] meets both requirements in a very efficient way.

The key to obtain a constant gm input stage lays in obtaining the correct tail current for each differential pair. Duque-Carrillo *et al.* technique is based on using a negative feedback loop to impose that:

$$gm_{REF} = gm_P + gm_N \tag{1}$$

where gm_{REF} is independent of the input common mode and gm_P and gm_N are the transconductances of the input differential pairs.

The negative feedback loop principle is illustrated in Figure 1. Here the differential pairs $T_{P,ref}$ and T_P are identical to the p-channel input stage differential pair, while T_N is identical to the n-channel one. All of them are unbalanced by a DC voltage V, small enough to ensure operation in the linear region. T_P differential pair is biased by a replica of the p-channel input stage differential pair tail current (I_{BP}) so it depends on the input common mode, but $T_{P,ref}$ is biased by a replica of the *nominal* p-channel tail current (I_B) and therefore it's gm is independent of the input common mode level. With the polarities shown in Figure 1 the differential output currents are added and the voltage of the summing node controls the T_N tail current (I_{BN}) as indicated by the dashed line. Doing so, the sum $i_{REF} + i_P + i_N$ always equals zero and using the small signal model for the differential pairs ($i = gm \times v_i$) we can easily obtain eq. (1).

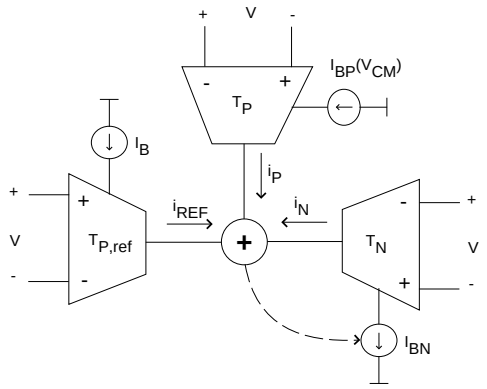


Figure 1. Schematic view of the constant gm operation principle.

Using a replica of I_{BN} to bias the actual n-channel differential pair of the input stage we will always have a common mode independent net transconductance in the input stage equal to gm_{REF}. Since $T_{P,ref}$ transconductance is independent of any matching conditions between n- and p-channel input transistors and their operating regions, the proposed architecture is both *robust* and *universal*.

Figure 2 shows the circuit implementation of the constant gm technique. The three differential pairs $T_{P,ref}$, T_P and T_N are shown. A folded cascode implements the summing circuit. This avoids deviations caused by the mismatch of the current mirrors that would be otherwise required to steer the currents to a summing node. Also, on the left of the circuit, there is a monitor circuit formed by a fourth differential pair whose transistors are identical to the p-channel input ones and with its drain and sources short-circuited. The gates are connected to the amplifier input signals, thus, sensing the input common mode and therefore always supplying T_P with the same common mode dependent tail current that bias the p-channel input differential pair.

3. Complete OpAmp Circuit

Having completed the input stage design we must now design the output stage of our amplifier. A cascode stage will be used to sum the currents of the input stage differential pairs while providing additional gain and a single high impedance node to drive the output stage.

The output stage must be able to drive different loads keeping at the same time a reduced power consumption. A class AB output stage presented by Silveira *et al.* [12] considerably reduces the output quiescent current consumption,

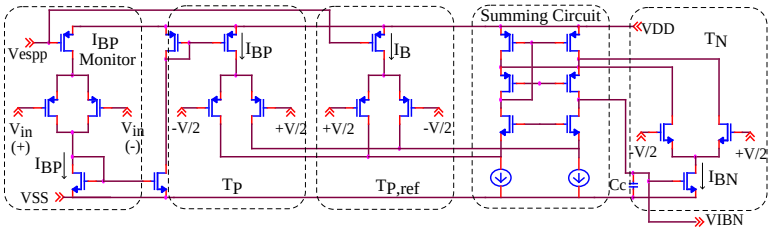


Figure 2. Implementation of the constant gm technique.

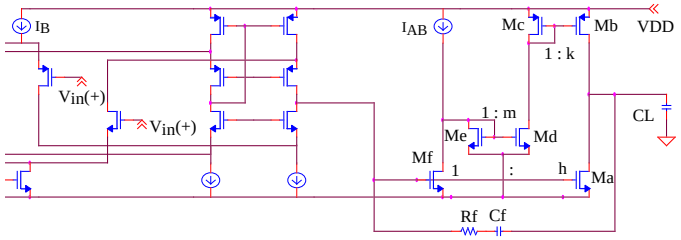


Figure 3. Opamp circuit implementation, omitting constant gm circuit.

with respect to an equivalent class A output stage. This is achieved by increasing the output stage transconductance to current ratio (gm/I_D) exploiting current gain through current mirrors. The new output stage transconductance is given by:

$$gm_{out} = gm_5(1 + \frac{km}{h})D(s) \quad (2)$$

where gm_5 is the transconductance of the output transistor M_5, k,m and h are the current mirrors gain factors as shown in figure 3 and $D(s)$ represents the contribution of the frequency response of the current mirrors. The factor $(1+\frac{km}{h})$ is noted as gm_{mult}

This output stage does not require extra compensating capacitances, is suitable for low voltage operation and is capable of driving loads that are up to the requirements of our reusable opamp. This output stage has already been successfully used in a very low power consumption ($100nA@2.0V$) pacemaker sensing channel application [13].

The complete opamp circuit schematic, omitting the constant-gm circuit shown in Figure 2, is shown in Figure 3.

4. Design Methodology

Design methodology is an important concern in this work. Design procedures and optimization algorithms were used in order to obtain minimum consumption while complying with the opamp requirements. Silveira *et al.* [14] presents a power optimization algorithm for a given settling time, that provides the optimum combination of slewing and linear settling periods over the total settling time. Also the optimum combination of the gm/I_D ratios of the input and output stages is obtained. In that work the algorithm was applied to a simple Miller OTA and proved to obtain a much better solution than those obtained with the application of fixed "rules of thumb".

In our work the algorithm was extended to our more complex architecture. To do so, the architecture was modelled at a higher level as a simple Miller OTA. The constant-gm input stage can be considered as a simple OTA input stage if frequency response of the cascoded summing mirrors is taken into account. The output stage class AB architecture can also be considered as a simple class A output transconductance as shown by Silveira *et al.*[12] by appropriate design. Under these conditions a RC compensation network is used to assure stability, as can be seen in Figure 3. The RC network eliminates the right half plane zero introduced by the Miller compensation, thus allowing to reduce the transconductance and hence the current needed at the output stage.

The Miller amplifier characteristics, modified to take into account our more complex architecture can be summarized with the following equations:

$$\omega_T = \frac{gm_T}{C_f} \quad (3)$$

$$\omega_{ndp} = \frac{gm_{out}C_f}{C_1C_2 + C_f(C_1 + C_2)} \quad (4)$$

$$PM = f(NDP, \omega_{13}, \omega_{15}, k, h, m, \omega_{fc}) \quad (5)$$

where ω_T is the transition frequency, ω_{ndp} is the Miller non-

dominant pole frequency, gm_T is the input stage net transconductance, C_f is the Miller compensation capacitance, gm_{out} is the output stage transconductance as given by (2), C_1 is the parasitic capacitance at the input of the output stage, C_2 is the load capacitance, PM is the phase margin, NDP is the ratio of ω_{ndp} over ω_T, ω_{13} and ω_{15} are the angular frequencies of the poles associated with the $M_{13} - M_{14}$ and $M_{15} - M_8$ current mirrors, k,h and m are the mirrors gains as explained in section 3 and ω_{fc} is the non dominant pole introduce by the folded-cascode stage.

The settling time expression given by Silveira *et al.* [14] is shown in (6).

$$t_s = \tau \left(\ln\left(\frac{1}{\epsilon}\right) - 1 + \ln(x) + \frac{1}{x} \right) \tag{6}$$

where $\tau = \frac{1}{\beta\omega_T}$, β is the amplifier closed loop feedback factor, ϵ is the output voltage relative error condition where settling time is defined and $x = \frac{\tau SR}{V_{step}}$, with V_{step} the amplitude of the step at the output of the amplifier and SR the slew rate.

The slew rate is approximated as in [14]:

$$SR = min(SR_1, SR_2) \text{ with } \begin{cases} SR_1 = \frac{I_{o1max}}{C_f} \\ SR_2 = \frac{I_{o2max}}{C_2} \end{cases} \tag{7}$$

where the amplifier slew rate is the minimum between the internal slew rate (SR_1) and the external slew rate (SR_2). Here I_{o1max} is the maximum current the folded cascode can provide, and is equal to I_B, where I_B is the input stage bias current. I_{o2max} is the maximum output stage output current and is equal to $gmmult \times I_{D5}$, where I_{D5} is the output transistor M_5 quiescent current.

Taking the more complex architecture into account, the design algorithm of the complete opamp integrates the output stage design algorithm presented in [12]. The following settling time driven, power optimization algorithm results:

1. Non-critical design parameters, as transistors length, or current sources gm/I_D ratios are chosen a priori by the designer. This parameters can be modified later, like for example, if the DC gain is not enough the transistor length can be increased.

2. The design space defined by the input and output stages gm/I_D is explored. The input stage gm/I_D its equal to the gm/I_D of the $T_{P,ref}$ differential pair transistors and will be noted as $(gm/I_D)_1$. Output stage gm/I_D can be obtained from equation (2) and depends on gm_5/I_{D5}, k, h, m and $D(s)$. For the space exploration gm_5/I_{D5}, noted as $(gm/I_D)_5$, will be used.

3. For each combination of these two parameters the compensation capacitor C_f is swept. For each value of C_f the amplifier is designed to comply with the total settling time specified, a given phase margin and the optimum class AB configuration. This is done by the following iterative process.

   (i) Initial values for I_{D5} and f_T are determined assuming $x = 0.5$, $NDP = 2.2$ and the simplified case where $C_1 \ll C_f \ll C_2$.

   (ii) The output stage power optimization routine is run. Optimum values for k,h,m and NDP are obtained.

   (iii) The rest of the circuit transistors are sized and capacitors C_1 and C_2 are calculated.

   (iv) x, f_T and I_{D5} are recalculated from the following equations derived from equations (2) to (7):

$$x = \frac{min\left[\frac{2}{(gm/I_D)_1},\ \frac{NDP(C_1C_2+C_f(C_1+C_2))}{(gm/I_D)_5 C_f C_2}\right]}{\beta V_{step}} \tag{8}$$

$$\omega_T = \frac{\ln(\frac{1}{\epsilon}) - 1 + \ln(x) + \frac{1}{x}}{\beta t_s} \tag{9}$$

$$I_{D5} = \omega_T \frac{NDP(C_1C_2 + C_f(C_1 + C_2))}{gm_{mult}(gm/I_D)_5 C_f} \tag{10}$$

   (v) If the relative difference with the initial values of f_T and I_{D5} is less than a given error then the process is finished, else we iterate at step 3ii with the calculated values of f_T and I_{D5}.

4. The value of C_f that gives the minimum total quiescent current consumption is determined.

When the complete algorithm is finished we obtain the value of C_f that minimizes the total current consumption for each point in the $(gm/I_D)_1$,$(gm/I_D)_5$ plane. The level curves of constant total consumption in this plane in a region around the optimum consumption can be seen in Figure 4 for the case of a design in $0.8\mu m$ CMOS technology, with the following data: $1\mu s$ of 1% total settling time at $0.3V$ step amplitude in follower configuration, 60 degrees phase margin with a $50pF$ load capacitance and $2V$ power supply. Additional results are shown in the following section.

All the algorithms were run in Matlab and the transistor model used in all calculations was the ACM model [3].

5. Results

In the conditions of the design from the last section, Table 1 shows the SPICE simulated characteristics of the opamp at different values of the reference current (I_{ref}). The data included are: transition frequency (f_T), phase

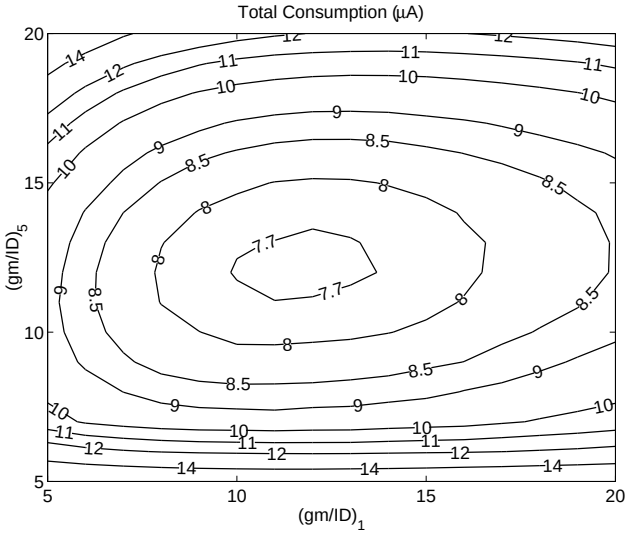


Figure 4. Constant total current consumption as a function of $(\mathbf{gm/I_D})_1$ and $(\mathbf{gm/I_D})_5$ ratios.

margin (PM), total current consumption (I_{DD}), settling time (t_{set}) and DC open loop gain (A_0). In this table we can appreciate how the amplifier can be tuned over more than 2 decades of f_T.

It might seem surprising the extremely high values achieved for the DC open loop gain. These are explained by several factors: a) there are three gain stages (the input stage, the cascode summing stage and the output stage), b) the output stage gain is enhanced by the transconductance multiplication effect, c) these values correspond to operation with a purely capacitive load, in which case the output stage gain is maximum, d) we are taking full advantage of the high gain achievable in the weak and moderate inversion regions. Nevertheless, it is expected to have smaller values in the experimental prototypes due to presence of parasitic and unmodeled effects in the transistor output conductance.

Figure 5(a) shows how the transition frequency and the phase margin varies with I_{ref} for 3 different input common mode levels. The increase in the phase margin for large I_{ref} is due to the fact that the f_T starts to fell behind and the frequency compensation isn't optimal. One of the reasons for this behavior is that for large I_{ref} many transistors in strong inversion go into triode region due to their high saturation voltages which does not fit in the low supply voltage. Figure 5(b) also shows the transition frequency and the phase margin, but in this case they are plotted against the input common mode voltage (V_{CM}). The figure clearly shows that the constant-gm circuit keeps the circuit optimally compensated through the entire input common mode range, even for large tuning currents.

Finally, Figure 6 shows how setlling time characteristic

Table 1. Calculated and Simulated characteristics of the designed opamp for 2V power supply voltage and 50pF load.

Params.	**Values**				
$I_{ref}(nA)$	0.2	2.4	40		135
			SPICE	MATLAB	
$f_T(kHz)$	7.5	75	790	770	1500
$PM(^o)$	60	62	68	>60	77
$I_{DD}(\mu A)$	0.04	0.5	8.2	7.9	27.3
$t_{set}(\mu s)$	184	19.7	1.4	1	0.91
$A_0(dB)$	137	157	162	>160	132

varies with the opamp tuning. The results with nominal operation ($I_{ref} = 40nA$) are slightly over the expected value (as can be seen also in Table 1), but the agreement achieved validates the methodology. Setlling time is also constant over the entire input common mode range, except when the input step pushes the common mode through the range where the constant-gm circuit has to steer the bias current from one pair to the other. In that case the delay introduced by this circuit increase the setlling time by a factor of 2 or 3. A more careful design of the constant-gm circuit could overcome this problem.

This amplifier is being fabricated at the time of submission of this article.

6. Conclusions

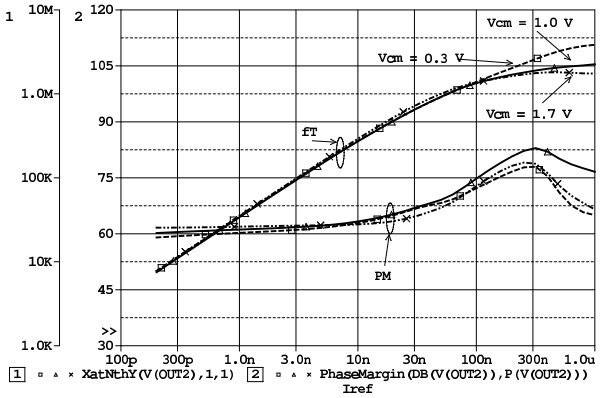
A recently proposed power optimization design methodology was extended to design a more complex architecture, including constant gm rail-to-rail input stages and a very low quiescent power class AB output stage. The power optimization algorithm for the output stage was also integrated, allowing to take full advantage of the benefits of this stage.

The results validate the original methodology and the extended one presented in this work. Results also confirmed that a reusable opamp for a wide range of applications was obtained.

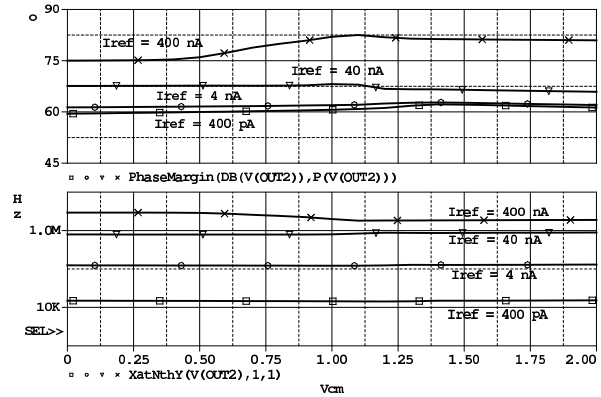
References

[1] R. Acosta, F. Silveira, and P. Aguirre. Experiences on analog circuit technology migration and reuse. In *Proc. XV Symposium on Integrated Circuits and Systems Design.*, pages 169–174. IEEE Computer Press, Sep. 2002.

[2] R. Castello. CMOS buffer amplifiers. In J. Huijsing, R. van de Plassche, and W. Sansen, editors, *Analog Circuit Design, Operational Amplifiers, Analog to Digital Conver-*



(a) Opamp tuning through I_{ref}, with different V_{CM}



(b) f_T and PM variation with V_{CM} for different I_{ref}

Figure 5. $\mathbf{fT}$ and Phase Margin behavior when the opamp is tuned from $\mathbf{I_{ref} = 0.4nA}$ to $\mathbf{I_{ref} = 400nA}$ and when input common mode level ($\mathbf{V_{CM}}$) varies.

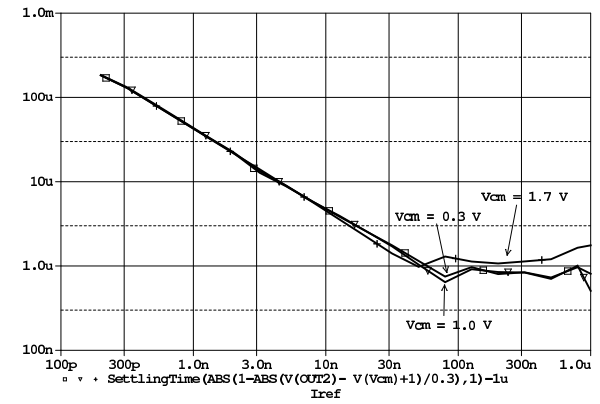


Figure 6. Setlling Time behavior when the opamp is tunned.

tors and Analog Computer Aided Design. Kluwer Academic Publishers, Dordrecht, 1992.

[3] A. Cunha, M. Schneider, and C. Galup-Montoro. An MOS transistor model for analog circuit design. *IEEE Journal of Solid-State Circuits*, 33(10):1510–1519, Oct. 1998.

[4] J. F. Duque-Carrillo et al. Robust and universal constant gm circuit technique. *Electronics Letters*, 38(9):396–397, April 2002.

[5] R. Hogervorst et al. CMOS low-voltage opeational amplifiers with constant gm rail-to-rail input stage. In *Proc. of the IEEE Int. Symp. on Circuits and Systems*, volume 6, pages 2876–2879, 1992.

[6] R. Hogervorst et al. A programable 3V CMOS rail-to-rail opamp with gain boosting for driving heavy resistive loads. In *Proc. of the IEEE Int. Symp. on Circuits and Systems*, pages 1544–1547, 1995.

[7] J. Huijsin and D. Linebarger. Low-voltage operational amplifier with rail-to-rail input and output ranges. *IEEE Journal of Solid-State Circuits*, SC-20:1144–1150, Dec. 1985.

[8] V. I. Prodanov and M. M. Green. Bipolar/CMOS (weak inversion) rail-to-rail constant-gm input stage. *Electronics Letters*, 33(5):386–387, Feb 1997.

[9] V. I. Prodanov and M. M. Green. New CMOS universal constant-gm input stage. In *Proc. of the IEEE Int. Conference on Electronics, Circuits and Systems*, volume 2, pages 359–362, 1998.

[10] W. Redman-White. A high bandwidth constant gm and slew-rate rail-to-rail CMOS input circuit and its application to analog cells for low voltage vlsi systems. *IEEE Journal of Solid-State Circuits*, 32(5):701–702, May 1997.

[11] S. Sakurai and M. Ismail. *Low-Voltage CMOS Operational Amplfiers*. Kluwer Academic Publishers, 1995.

[12] F. Silveira and D. Flandre. Analysis and design of a family of low-power class AB operational amplifiers. In *Proc. XIII Symposium on Integrated Circuits and Systems Design.*, pages 94–98. IEEE Computer Press, Sep. 2000.

[13] F. Silveira and D. Flandre. A 110nA pacemaker sensing channel in CMOS on silicon-on-insulatator. In *Proc. of the IEEE Int. Symp. on Circuits and Systems*, volume V, pages 181–184, 2002.

[14] F. Silveira and D. Flandre. Operational amplfier power optimization for a given total (slewing plus linear) settling time. In *Proc. XV Symposium on Integrated Circuits and Systems Design.*, pages 247–253. IEEE Computer Press, Sep. 2002.