Experiences on Analog Circuit Technology Migration and Reuse.

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Abstract

This work deals with two aspects of the reuse and redesign of analog circuits. First, a method for technology migration of analog circuits, recently proposed by Galup-Montoro and Schneider, is validated experimentally in the redesign of a Miller OTA from a 2.4µm technology to a 0.8µm technology. In addition, the impact of the method on performance aspects of analog circuits not covered in the original proposal (slew rate and current mirror frequency response) is studied. As a second mechanism for allowing the reuse of analog circuits, the feasibility of the application of the reference bias current as a tuning parameter to customize the performance of an existing design to suit different applications is demonstrated.

1. Introduction

The reuse of circuit designs is an essential tool to comply with shrinking time to market requirements in integrated circuits that at the same time increase in complexity to implement systems on a chip. The urge for implementing reuse capabilities is particularly intense in the analog field [1]. Automatic synthesis of analog circuits is a much hard problem than for the digital counterparts, due to the larger number of variables and interactions. Hence, analog automatic synthesis is much less developed than digital synthesis, further increasing the demands for experienced designer time in the analog field.

The reuse of circuit designs involves several aspects. One is technology migration, as one system or block changes the fabrication process, for example to exploit the benefits of scaled technologies for digital circuits. Other is the capability to apply a given circuit design to operate in different systems in the same technology, with necessarily changing performance or environmental (e.g. loading impedance) conditions.

The need for solutions to these problems has recently started to be addressed at the academic and commercial level, particularly the one of technology migration. References [2, 3] and [4] deal with the issue of technology scaling. Some companies [5] have recently started to offer tools and services aimed at reuse and technology migration. The approach of reference [4] and those of company [5] have in common that they base their approaches on some kind of optimization loop that varies circuit parameters (e.g. transistor sizes and currents) coupled with intensive SPICE simulations that check the compliance with the specified performances. These approaches have the drawback of being "blind" procedures that are not able to take advantage of a careful optimization of design trade-offs that an skilled designer might have done in the original design. They also do not take into account the evolution of analog circuit performance aspects with scaling, and thus a priori do not exploit the advantages that might arise (e.g. the opportunity to move the operation point towards weak inversion).

The method proposed in [2,3] is analytical and makes it possible to study the evolution of the different circuit aspects and choose the best strategy. References [2,3] presented only simulation results as support for the proposed methodology. In this work we present experimental results of the application of the method proposed in [2] to a complete Miller OTA. In addition, we extend the analysis done in [2] to include additional performance aspects of analog circuits (slew rate and the current mirror frequency response).

Other aspect of the reuse of analog circuits is also analyzed in this work. It refers to the possibility of programming or "tuning" the circuit performance in order to suit different applications. The application of bias current tuning is analyzed for the migrated Miller OTA.

The paper is organized as follows. Section 2 briefly summarizes the method presented in [2], highlights how it was applied to our circuit and discusses the evolution of additional performance parameters not covered in [2] with scaling. In section 3, the analytical results of the redesign of a Miller OTA from a 2.4µm to 0.8µm and 0.35µm technologies together with the experimental results obtained for the 2.4µm and 0.8µm technologies are presented. Section 4 discusses the application of bias

current tuning to this amplifier and Section 5 summarizes the main conclusions.

2. Redesign method based on the ACM model.

This work is based on the resizing rules [2] resulting from the application of the ACM (Advanced Compact Model) [6] model of the MOSFET transistor.

The nMOS transistor equations in saturation in the ACM model are given by:

$$I_D = I_S \cdot i_f$$

where I_D is the drain current; I_S is a normalization current defined by $1/2\,\mu_n n C_{OX} U_T^2 (W/L)$, with μ_n the mobility, n the slope factor, C_{ox} the gate oxide capacitance per unit area, U_T the thermal voltage and W/L the transistor aspect ratio; and *if* is a normalized current associated with the level of inversion at the source of the transistor that verifies:

$$\frac{(V_G - V_{T0})}{n} - V_S = U_T \cdot \left(\sqrt{1+i_f} - 2 + \ln\left(\sqrt{1+i_f} - 1\right)\right)$$

where V_G and V_S are the gate and source voltage referred to the substrate, V_{T0} is the threshold voltage at zero V_S and n is the subthreshold slope factor.

The gate transconductance to drain current ratio is given by:

$$\frac{g_m}{I_D} = \frac{1}{nU_T} \cdot \frac{2}{\left(\sqrt{1+i_f} + 1\right)}$$

From these equations the redesign rules are obtained [2]. The migration of technology implies the change of some parameters, as a result the following scaling factors are defined.

$$V_{DD\,2} = \frac{V_{DD\,1}}{K_V}$$

$$C_{OX\,2} = C_{OX\,1} \cdot K_{COX}$$

$$\mu_2 = \frac{\mu_1}{K_\mu}$$

$$L_{min\,2} = \frac{L_{min\,1}}{K_L}$$

$$V_{E1} = V_{E2} \cdot K_E$$

where VDD is the supply voltage, Lmin is the minimum transistor length of the technology, VE is the Early voltage that defines the small signal drain conductance, and subscripts 1 and 2 refer to the initial and target technology. Factors K are defined such that they are greater than 1 when technology 2 is a down scaled version of technology 1.

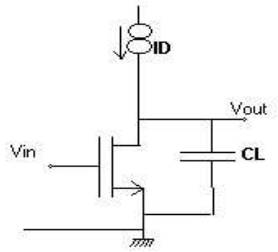

Figure 1. Common Source Configuration

In article [2], the redesign rules are derived considering the case of a MOSFET in a common source configuration (Fig. 1). They are built so that the technology migration preserves constant the following performance data: the stage gain-bandwidth product, the maximum signal to noise ratio and the transistor's transition frequency.

Two scaling strategies are analyzed in [2], channel length scaling and constant inversion level scaling. The most convenient proves to be the first one, particularly from the point of view of taking advantage of technology scaling to reduce power consumption. Applying this strategy, the redesign rules proposed in [2] are summarized in Table 1. In some rows of Table 1 the limit cases that result when the transistor operates in weak inversion (WI) and strong inversion (SI) are shown to provide easily tractable results. Nevertheless the proposed method is general, allowing to determine the scaling factor for any inversion level.

Table 1. Rules and results of channel length redesign as proposed in [2].

	WI	SI
V_{DD}	$1/K_V$	
Capacitances (Gate and Load)	K_V^2	
L	$1/K_L$	
W	$K_L.K_V^2/K_{Cox}$	
g_m	K_V^2	
i_f	$\sqrt{1+i_{f2}} - 1 = \frac{K_\mu}{K_L^2}\left(\sqrt{1+i_{f1}} - 1\right)$	
	K_μ/K_L^2	K_μ^2/K_L^4
I_D	K_V^2	$(K_\mu/K_L^2).K_V^2$
Power	K_V	$(K_\mu/K_L^2).K_V$
DC gain	K_E/K_L	$K_E.K_L/K_\mu$
Area	K_V^2/K_{Cox}	

We will now analyze the evolution of two parameters of interest for analog design when these rules are applied.

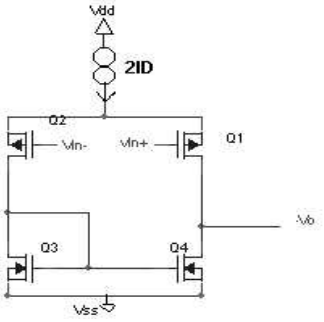

Figure 2. Differential amplifier

They are the slew rate of a common source MOSFET configuration and the pole frequency of a current mirror.

The slew rate of the common source amplifier of Fig. 1 is given by:

$$SR = \frac{I_D}{C_L}$$

If weak inversion is considered, then

$$I_{D2} = K_V^2 \cdot I_{D1} \text{ and } C_{L2} = K_V^2 \cdot C_{L1}$$

As a result, in weak inversion

$$\frac{I_{D2}}{C_{L2}} = \frac{I_{D1}}{C_{L1}}$$

and the SR remains the same. Proceeding in analog way for strong inversion, results that the SR decreases by the factor (K_μ/K_L^2). In moderate inversion an intermediate situation arises. Therefore care must be taken on the evolution of this parameter since it tends to worsen with this scaling strategy.

In the method proposed in [2], the size and current of all transistors of the circuit are scaled with the same set of rules. However, when we have a differential amplifier as the one shown in Fig. 2, the current through the current mirror transistors is linked to the one through the differential pair. Then the scaling of the current mirror transistors current is fixed by the scaling of the differential pair current to keep the overall amplifier gain bandwidth constant. Therefore the current mirror scaling will not follow all the rules proposed above and will not keep constant the g_m/C ratio that defines the current mirror pole.

Considering the rules for the scaling of L,W, μ and Cox the current mirror pole changes as:

$$\frac{\omega_{pole2}}{\omega_{pole1}} = \frac{K_L^2}{K_\mu}\left(\frac{\sqrt{1+i_{fM2}}-1}{\sqrt{1+i_{fM1}}-1}\right)$$

where if_{M2} and if_{M1} are the inversion level of the current mirror transistors in technology 2 and 1.

Considering the rule for *if* of the differential pair (if_P), given in Table 1, the relationship between if_P and if_M is:

$$\sqrt{1+\frac{i_{fP1}}{i_{fM1}}i_{fM2}}-1 = \frac{K_\mu}{K_L^2}\left(\sqrt{1+\frac{i_{fP1}}{i_{fM1}}i_{fM1}}-1\right)$$

From these last equations it is possible to predict the behavior of the pole frequency after the redesign. Fig. 3 shows that if $if_{P1}/if_{M1}<1$, the pole frequency grows and the current mirror improves its performance. This is usually the case since due to matching considerations, the current mirror tends to be designed with a higher inversion level than the differential pair.

3. Redesign of a micropower Miller amplifier

The redesign of a micropower Miller OTA was calculated, simulated and experimentally tested on silicon. The example chosen comes from an industrial application. It is part of a sense channel of an implantable cardiac pacemaker, where it is applied to amplify and filter the cardiac signal to then determine whether the heart has

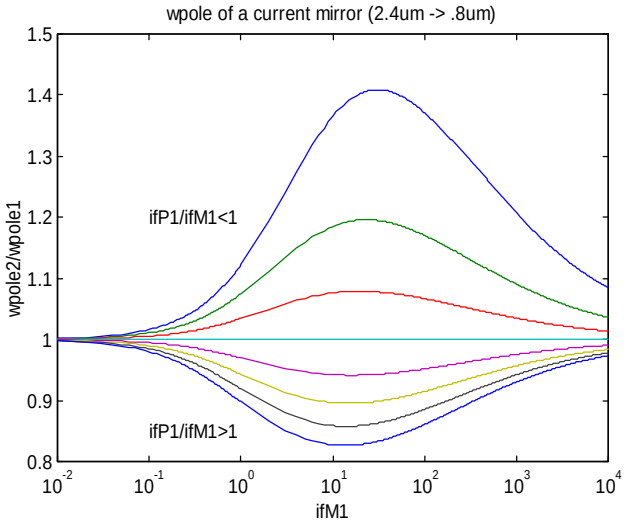

Figure 3. Evolution of current mirror pole frequency as function of the ratio between the differential pair inversion level and the current mirror inversion level in the original design, when this ratio changes from 0.25 to 4.

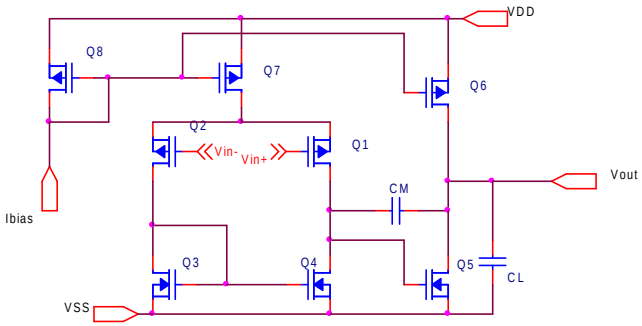

Figure 4. Schematic of redesigned Miller OTA

spontaneously contracted. In this system the amplifier is applied with a fixed high closed loop gain. Thus it is not required that it would be stable in unity gain configuration. Therefore, as a mean to save consumption, and allowing for wide security margins, the amplifier was designed to have a 60-degree phase margin for a 20dB closed loop gain. This circuit was designed in a 2.4µm technology and must handle a 50pF load and operate from implantable device batteries from supply voltages of 2.8V down to 2V. Fig. 4 shows the amplifier schematic diagram.

The redesign methodology proposed in [2] was applied to this amplifier, re-targeting it for 0.8µm and 0.35µm technologies. In addition, the resulting design in the 0.8µm technology was fabricated and tested. Since the intended application (implantable devices) has a fixed supply voltage determined by the used batteries, the redesign was done keeping fixed the supply voltage (KV=1). The rest of the scaling factors were as follows: 0.8µm technology: KCox=2.56, KL=3.75, KEn (KEp) = 5.52 (2.78), Kµn (Kµp) = 1.29 (1.50); 0.35µm technology: KCox=5.47, KL=8.57, KEn (KEp) = 10 (6), Kµn (Kµp) = 1.60 (1.92). Table 2 compares the calculated amplifier characteristics in each of the technologies.

Table 2. Calculated results.

	2.4µm	.8µm	.35µm
DC gain (dB)	77.7	83.0	79.7
f_T (kHz)	57.2	58.7	56.9
Phase margin (°)	19.4	19.5	19.3
Frequency at 60° phase margin (kHz)	13.2	13.3	13.0
Open loop gain at 60° phase margin (dB)	19.9	19.9	20.1
Power (µW)	1.54	1.43	1.42
SR (V/ms)	8.0	7.63	7.33
Area (mm^2)	.0166	.0072	.0046

Simulation results are compared in Fig. 5 for the three technologies. Experimental results are compared in Fig. 6 and Table 3 for the 2.4µm and the 0.8µm technologies.

Table 3. Measured characteristics of the original and the automatically scaled design.

	2.4µm	0.8µm
Gain Bandwidth (kHz)	59.15	59.50
DC Gain (dB)	78.4	85.3
Phase Margin (°) @13.2 kHz	65.5	54.2
Offset voltage (mV)[1]	7	9
Power (µW)	1.7	1.51

From these results, the very good performance of the scaling method can be appreciated. The parameter that presents a larger spread is the DC gain. This was expected since this parameter depends on the ill modeled and highly variable output conductance. Though only one sample was characterized to this regard, the offset is similar in both technologies.

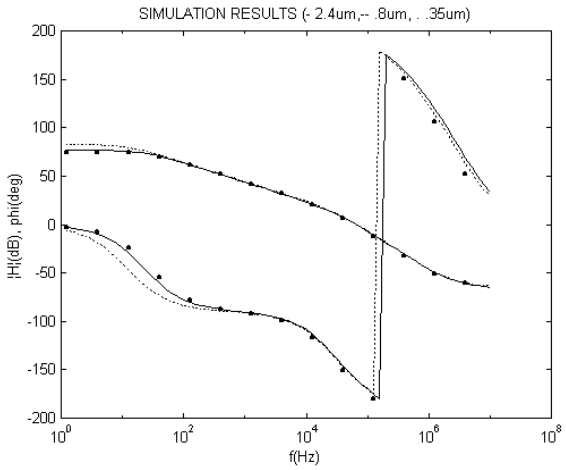

Figure 5. Comparison of simulation results between original (2.4µm, solid line) and scaled designs (0.8µm, dashed line and 0.35µm, dots).

1 Measurement result for only one sample.

Table 4. Performance comparison between SPICE simulation and calculated results.

Iref (nA)	4,34		43,4		434	
Source	Calc.	SPICE	Calc.	SPICE	Calc.	SPICE
A (dB)	81,2	79,47	80,46	79,19	78,18	78,46
f @ 20dB gain (kHz)	1,31	1,43	12,5	13,46	109,51	119,14
PM @ 20dB gain (°)	66,26	61,78	66,27	61,98	66,35	62,26
Input Common Mode Range Max (V)	1,25	1,4	1,15	1,31	1,02	1,2
Input Common Mode Range Min (V)	0,17	0,13	0,17	0,13	0,17	0,14
Output Swing Max (V)	1,85	1,92	1,84	1,9	1,81	1,87
Output Swing Min(V)	0,15	0,09	0,15	0,09	0,16	0,09
SR (V/ms)	0,76	0,73	7,63	7,24	76,29	72,25
Equivalent input noise spectral density Vn@ f=100Hz (uV/sqrt(Hz))	5,58	4,39	3,01	2,44	1,79	1,45
Offset (mV)	4		3,99		3,95	

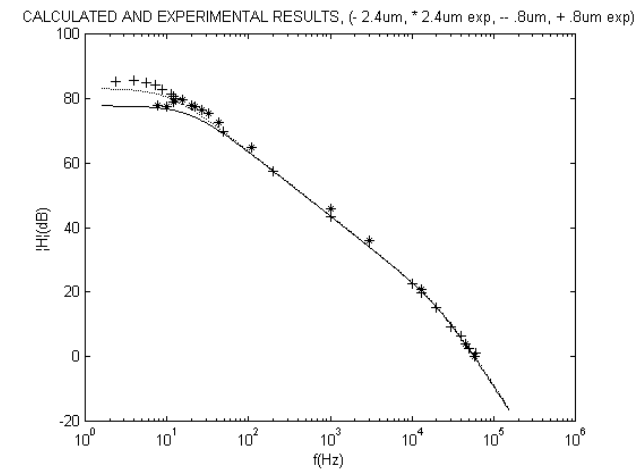

Figure 6. Comparison of calculated and measured open loop frequency response for original and scaled design. The following curves are shown: calculated 2.4μm design (solid line); calculated 0.8μm (dashed line); measured, 2.4μm design (star symbols) and measured, 0.8μm design (plus symbols).

4. Amplifier reuse through bias current tuning

This section evaluates the feasibility of applying the reference bias current of the whole amplifier as an adjustment parameter to tune an existing amplifier performance to suit different applications and hence save design time.

The essential issue is that the exponential dependence of current on voltage in the weak and moderate inversion regions, implies a very low dependence on gate voltage on current and is also reflected on a flat g_m/I_D versus I_D curve, and a quasi constant saturation voltage. Then, a design in these regions of operation of the MOS transistor can have the speed (gain bandwidth, slew rate) versus consumption trade-off customized by changing the reference bias current for all the design while preserving acceptable operation in all the other aspects (input common mode range, output swing, phase margin, ...).

This was verified through simulations of the amplifier redesigned for 0.8μm technology in Section 4. Table 4 compares the calculated performance and the SPICE simulation results applying the BSIM3v3 model with parameters supplied by the foundry. The supply voltage is 2V.

5. Conclusions

The redesign rules proposed in [2] were applied in a micropower Miller OTA. Calculation, simulation and experimental results were checked against the original design. The results experimentally support the validity of this redesign technique. The impact of the redesign method on two additional performance aspects (slew rate and current mirror frequency response) was analyzed. The results show that the proposed method decreases the slew rate and hence this is an aspect to look after in the resulting design. Regarding the current mirror frequency response, our analysis show that if the current mirror transistors were originally designed to work in stronger inversion than the differential pair transistors, the current mirror pole

frequency increases, preserving a good overall frequency response.

Finally, the possibility of applying the bias current as a tuning parameter to customize an existing design for different applications was analyzed. The simulation results confirm that for weak and moderate inversion designs, this approach works very well in various orders of magnitude of bias current, and, hence, transition frequency and slew rate values.

6. References

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