Ultra-low Power CMOS Cells for Temperature Sensors

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ABSTRACT

Temperature sensors and voltage references require cells that generate both PTAT (Proportional To Absolute Temperature) and NTC (Negative Temperature Coefficient) voltages. We present a novel theoretical approach based on a quasi-constant current to obtain these voltages in standard CMOS technology using *no resistors*. A test circuit was fabricated in a 0.8 μm CMOS process. We performed measurements in a 305 K to 375 K temperature range which verify the expected results. The circuit draws under 50 nA from a 1.6 V to 3.0 V supply.

Categories and Subject Descriptors

B.7.m [**INTEGRATED CIRCUITS**]: Miscellaneous

General Terms

Design

Keywords

Temperature Sensor, Voltage reference, Current reference, CMOS, Micropower

1. INTRODUCTION

The current state of electronic systems design allows the integration of an increasing number of circuits in a single chip, making systems-on-chip (SoCs) a reality.

A wide spectrum of applications benefit from the inclusion of sensing functionality in SoCs. Particularly, as temperature is a key measurement in many SOCs, temperature sensor cells have become a basic building block in state of the art Integrated Circuit (IC) design.

Temperature sensing cells are used in a wide range of applications: biomedical, cold chain monitoring and industrial applications to name just a few. Many of these applications are intended for use in portable or even implantable systems with very long battery life.

The main goal of our research is to achieve the minimum possible consumption while low voltage operation is also a desirable characteristic. The desired precision is around 0.5 K, for a temperature range from 230 K to 400 K, except in the case of biomedical applications where the temperature range is much limited but the precision should be around 0.05 K.

We researched ways to obtain basic PTAT and NTC cells for our temperature sensors. In [1] we detail the theory behind the cells and provide simulation results in the 230 K to 400 K range. The present work reviews the main results and introduces measurements which validate them.

The paper is organized in the following way. Section 2 introduces the notation while reviewing the basic MOS models upon which we base our derivations. Section 3 presents the theoretical basis for the cells we propose. The circuit of the fabricated prototype is presented in section 4. The measurements on this circuit are reviewed in section 5. Finally, we summarize our conclusions in section 6.

2. NOTATION

The following notation will be used throughout this paper.

Temperature relative to an arbitrary reference (often, $T_R = 300\,K$) will be denoted as

$$x = \frac{T}{T_R} \tag{1}$$

The R subscript will be applied to any variable taken at the reference temperature.

We will use the following notation for the thermal voltage:

$$U_T = \frac{kT}{q}, \qquad U_{TR} = \frac{kT_R}{q} \tag{2}$$

The usual models for MOS transistors are used for the different operating regions. These equations, included here for reference purposes, are expressed in terms of the pinch-off voltage V_P and the form factor S:

$$V_P = \frac{V_G - V_T}{n}, \qquad S = \frac{W_{eff}}{L_{eff}} \tag{3}$$

In weak inversion (WI) the drain current is

$$I_D = 2Sn\mu C_{ox}U_T^2 e^{\frac{V_P}{U_T}} \left[e^{-\frac{V_S}{U_T}} - e^{-\frac{V_D}{U_T}} \right] \tag{4}$$

In saturated strong inversion (SI,sat):

$$I_D = \frac{1}{2}Sn\mu C_{ox}V_P^2, \qquad V_S = 0 \tag{5}$$

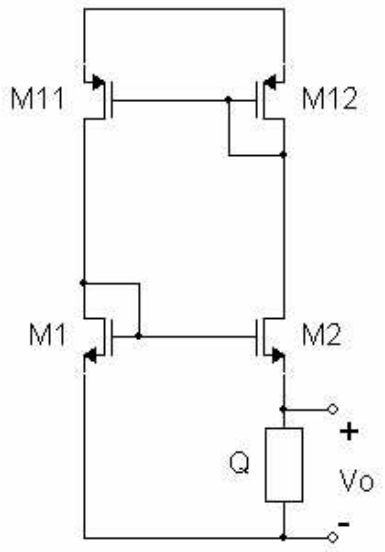


Figure 1: CMOS implementation of Classical PTAT Circuit

and for linear strong inversion (SI,lin):

$$I_D = Sn\mu C_{ox} V_D \left(V_P - \frac{V_D}{2} \right), \qquad V_S = 0 \tag{6}$$

Besides, we will consider first order variations of the threshold voltage (V_T) with temperature:

$$V_T = V_{TR} + k_{VT}(x-1), \qquad k_{VT} < 0 \tag{7}$$

and the usual equation for the temperature dependence of mobility:

$$\mu = \mu_R \, x^{k_\mu}, \qquad k_\mu < 0 \tag{8}$$

3. THEORETICAL BACKGROUND

The most ubiquitous circuit, both in temperature sensors and voltage references, is the PTAT (Proportional To Absolute Temperature) circuit [3–5, 9]. Usually implemented with a pair of bipolar transistors biased at different current densities, it can be implemented with MOSFETs biased in weak inversion as well (Fig. 1) [7].

In both cases the carrier transport is dominated by diffusion phenomena, and thus, they obey similar exponential equations.

The output voltage of the PTAT cell in Fig. 1 is

$$V_o = \alpha_T \, U_T = x \, \alpha_T \, U_{TR}, \qquad \alpha_T = \ln(AB) \tag{9}$$

where $I_{D1} = AI_{D2}$ and $S_2 = BS_1$.

It must be noted that Vo does not depend on I_{D1} and I_{D2} and therefore it does not depend, to some extent, on the nature or value of the element Q.

The element Q determines the branch currents. For micropower applications, if Q is a resistor, its resistance must be very high which implies spending a huge area. Besides, the temperature dependence of the resistance is in general poorly known [6].

We have researched several options for the bias fixing element Q [1]. Our best choice is the circuit proposed by Oguey *et al.* [6] (Fig. 2) in which Q is a non-saturated SI MOS (M4) biased by an auxiliary branch.

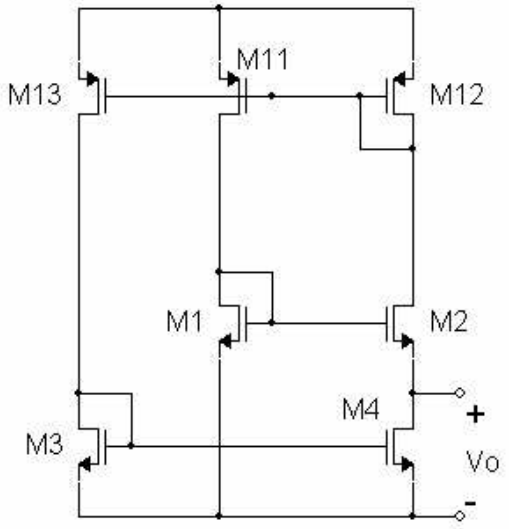


Figure 2: PTAT biasing through an MOS (SI,linear)

In this circuit the current through M4 presents the following temperature dependence:

$$I_4 = I_{4R} \, y(x) \, x^{k_\mu + 2} \tag{10}$$

where

$$y(x) = \frac{n(x)}{n_R} \tag{11}$$

is the relative variation of the slope factor n with temperature and I_{4R} is the value of I_4 at some arbitrary reference temperature.

Expression of I_{4R} as a function of geometrical and technology parameters yields design equations which we have thoroughly reported in [1]. Proper sizing of M3, M4 and M13 allows us to independently choose I_{4R} and V_{G4R}.

For usual dopant concentrations and in the temperature range we are interested in, the theoretical value for the mobility exponent is $k_\mu = -1.5$ [10] while $k_\mu = -1.8$ for the technology of our prototypes. Besides, $y(x)$ varies just $\pm 5\%$ in a 200 K to 400 K range. Thus, I_4 has a weak temperature dependence and can be used as a *quasi-constant current* to bias not only the embedded PTAT source but other circuits as well.

In [1] we have introduced the idea of using the above defined quasi-constant current in the following circuits obtaining some interesting results.

3.1 Diode Connected MOS

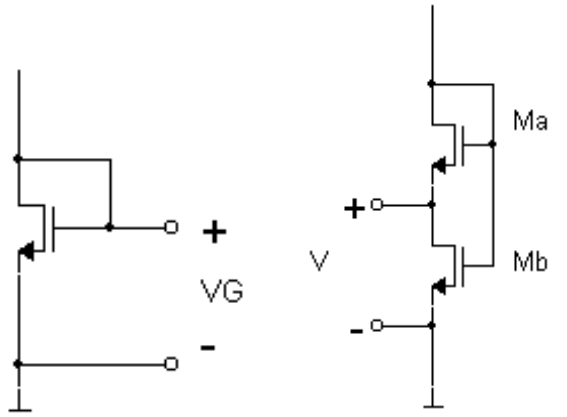
Considering first order variations in V_T (Eq. 7), a diode connected MOS (Fig. 3(a)) operating in WI and biased with the quasi-constant current of Eq. 10 yields a gate voltage (Fig. 4):

$$V_G = V_0 + x \, \left[k_{VT} + y(x) \, (V_{GR} - V_{TR}) \right] \tag{12}$$

where

$$V_0 = V_{TR} - k_{VT} \ , \tag{13}$$

$y(x)$ was defined in Eq. 11 and V_{GR} is the value of V_G at the reference temperature. V_{GR} depends on the size of the MOS transistor [1].



(a) Diode connected MOS. (b) MOS voltage divider.

Figure 3: MOS circuits

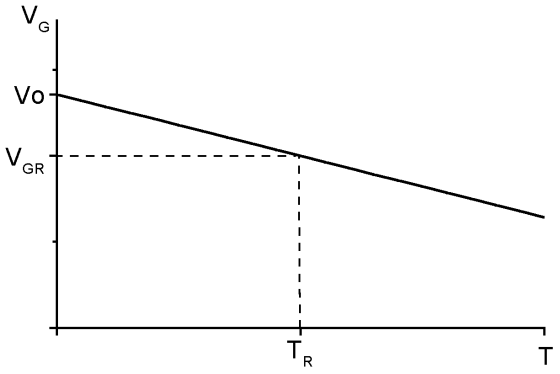


Figure 4: Temperature dependence of Voltage across Diode-connected MOS

If the diode connected MOS is operated in SI, the same first order temperature variation holds true, although the dependence of V_{GR} with technology and geometrical parameters is different [1].

As mentioned above, $y(x)$ has a weak temperature dependence throughout the temperature range, thus Eq. 12 is close to a straight line. V_{GR} fixes the slope of Eq. 12 which, in SI, can be chosen to be positive, negative or zero.

A negative slope is useful as a complement to PTAT circuits for temperature sensing as proposed in [1]. A zero slope can be used as a reference voltage. In this case, as both the reference value and the slope depend on technology parameters a calibration means must be provided. As far as we know, these results have been recently introduced by the authors in [1].

3.2 MOS Voltage Divider:

Fig. 3(b) shows a MOS voltage divider formed by transistors Ma and Mb. Both transistors have the same width but different lengths. We define the following relationship between the length of transistor Mb (Lb) and the sum of both transistor lengths ($L = La + Lb$):

$$L_b = \alpha L \tag{14}$$

It is already known that when the divider operates in WI, its lower section displays a PTAT voltage [8]:

$$V = x\, V_R \tag{15}$$

with

$$V_R = U_{TR}\ \ln\left(\frac{1}{1-\alpha}\right) \tag{16}$$

It can be shown that in SI the drain-source voltage in transistor Mb is:

$$V = \left(1-\sqrt{1-\alpha}\right)\frac{V_G - V_T}{n} \tag{17}$$

which allows us to extend the above result as follows [1]: When biased with the quasi-constant current I_4 (Eq. 10), V_G is such that Eq. 15 also holds true:

$$V = xV_R \tag{15}$$

but now

$$V_R = \left(1-\sqrt{1-\alpha}\right)\sqrt{\frac{2I_R}{Sn_R\mu_R C_{ox}}} \tag{18}$$

4. TEST CIRCUIT

We combined some of the previous subcircuits in a comprehensive cell which generates several voltages with the main purpose of checking the results we present in Section 3. It also implements a current source to be used in a ramp generator, which was also designed but lies outside the scope of this paper.

The circuit is shown in Fig. 5 and was designed taking $T_R = 300\,K$ as the reference temperature.

The core of the circuit is formed by M1 to M4 as in Fig. 2. M1 and M2 operate in WI, while M3 and M4 are in SI (M4 is not saturated). The main purpose of the core is to generate the quasi-constant current (Eq. 10) which biases the whole circuit through the cascoded current mirror implemented by PMOS transistors M11 through M28.

V_{p1} is a PTAT voltage (see also Fig. 1) which displays a small slope ($V_{p1R} = 53.8\,mV$).

As M3 is in SI and biased by the quasi-constant current its gate voltage is that of Eq. 12. For research purposes we designed for $V_{n3R} = V_0$ (see Eq. 13, $V_0 = 1.23\,V$). This way, we achieve a constant voltage reference (uncorrected for curvature effects) in a circuit with no resistors. Below we will show that this can be done even at very low currents, which extends its usefulness to micropower systems.

V_0 is directly related to process parameters presenting strong variations, mainly V_T. This is a disadvantage when comparing this circuit to traditional bipolar or BiCMOS "bandgap" circuits because, in the latter, the equivalent to V_0 is fixed by a material related constant.

M3, an MOS in SI biased with the quasi-constant current, was split in two serial transistors M3A and M3B implementing the divider of Fig. 3(b) which fulfills Eq. 15. This way we generate the PTAT voltage V_{p3} which can be easily designed with higher sensitivity than V_{p1}. ($V_{p3R} = 268\,mV$ for our test circuit)

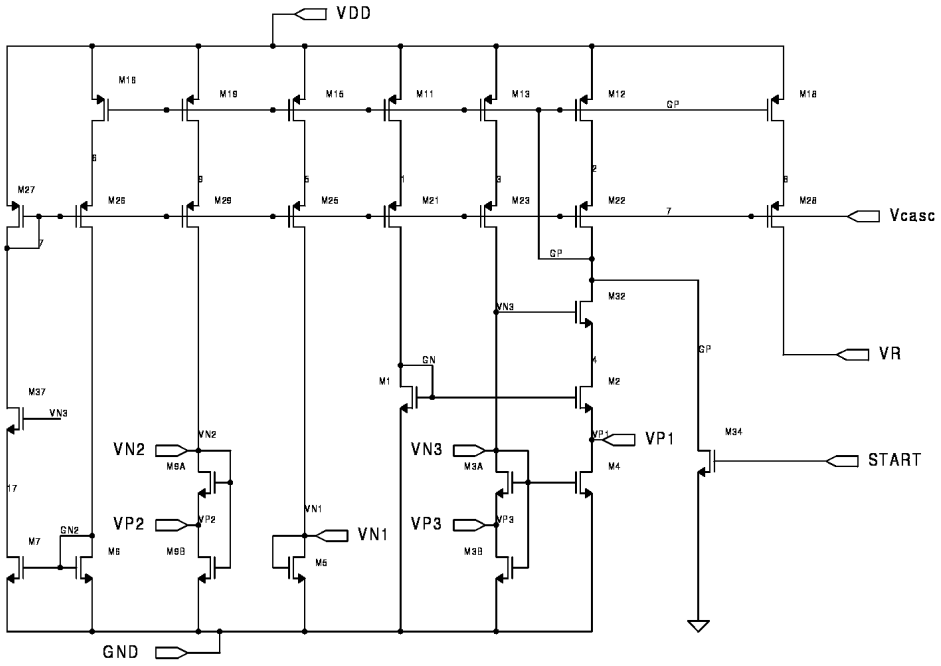


Figure 5: Complete cell schematic

To avoid disturbances in the bias generating core when measuring V_{n3} or V_{p3}, we replicated M3 on branch 9 (M9A, M9B, M19, M29), generating V_{n2} and V_{p2} ($V_{n2R} = V_{n3R}$, $V_{p2R} = V_{p3R}$). We still split M3 for better matching with the replica M9.

Branch 5 (M5, M15, M15) biases the diode connected MOS M5 in WI, thus generating V_{n1} (Eq. 12) which displays a negative dependence with temperature. ($V_{n1_R} = 556mV$)

In this circuit, any mismatch has the effect of changing one or more parameters of the output voltages. This is no worse than the parameter uncertainty due to technology parameter spread. Both effects have to be dealt with by proper calibration.

System considerations related to the ramp generator led us to using cascoded mirrors [2]. This has the added advantage of minimizing the influence of the power supply (V_{DD}) on our circuit. Auxiliary branches 6 and 7 generate the gate voltage of the cascode transistors. We decided to operate these branches with 1/5 the current of the others to keep the overall consumption low.

5. EXPERIMENTAL RESULTS

The test circuit was fabricated on a standard $0.8\mu m$ CMOS technology. Fig. 6 shows a microphotograph of the circuit, which has an area of $(465 \times 210)\mu m^2$.

Four samples (chips A-D) were tested, measuring outputs $V_{p1}, V_{p2}, V_{n1}, V_{n2}, V_{n3}$ and chip consumption I_{DD} at several combinations of ambient temperature and supply voltage V_{DD}.

Chips B and C were swept from 305 K to 400 K (aprox. 32^oC to 127^oC) while chips A and D were limited to 375 K. These tests were performed in a custom built oven under computer controlled temperature achieving an error of ± 10 mK.

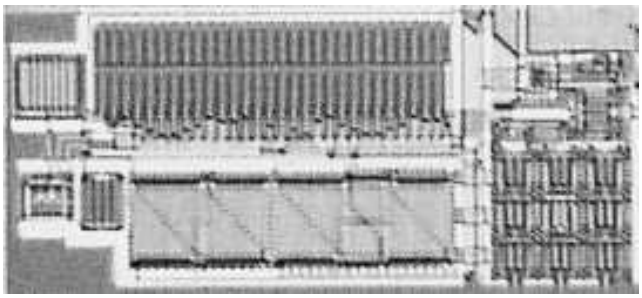


Figure 6: Microphotograph of the fabricated cell.

All chips worked correctly with negligible output variations for $1.6\,V \leq V_{DD} \leq 3.0\,V$ as predicted by simulations. Therefore, we only present results obtained at $V_{DD} = 3.0\,V$ which are representative of the behaviour through the whole supply operating range.

Current through the power supply (I_{DD}) is proportional to the branch currents (I). As no current flows through branch 8 (M18, M28), the PMOS current mirror determines $I_{DD} = \frac{27}{5}\,I$

Fig. 7 shows I_{DD} as a function of temperature for each sample. The expected quasi-constant current model holds true up to 350 K, exponentially departing from it thereof. We traced this misbehaviour to leakage currents, mainly in the drain and source areas of M1 and M2.

Fig. 8 depicts measured voltages as a function of temperature. We present voltage data for the full temperature

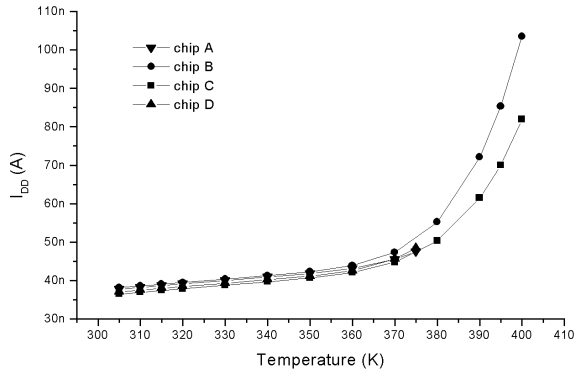


Figure 7: Current consumption for the 4 measured prototypes as a function of temperature.

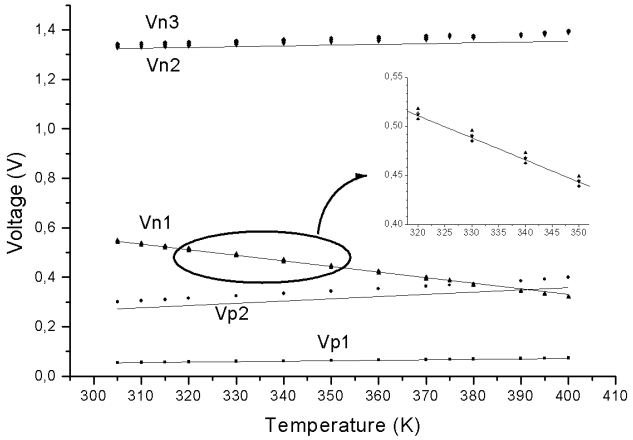


Figure 8: PTAT and NTC voltages for 4 prototypes. The solid lines show the behaviour predicted by the model for each voltage. The inset shows a detail of V_{n1}.

range. However some departure from the predicted values is expected for $T > 350\,K$ due to the effects of the increased leakage currents. Experimental data are presented as dots while lines show the values predicted by our theoretical model. The latter values are computed using parameters estimated from measurements performed by the foundry on the prototype wafer. As the temperature dependence of the threshold voltage (k_{VT} , Eq. 7) was not reported by the foundry, we used the value from the technology data sheet. The variation of slope factor with temperature $y(x)$ (Eq. 12) was approximated as $y(x) = 1$

As Fig. 8 and its inset show, V_{p1} and V_{n1} data are in excellent agreement with theory. V_{p2} is quite sensitive to small variations in geometrical parameters which explains some difference between measured data and theory.

The theoretical curve for V_{n2} and V_{n3} depends on n and k_{VT} which were either just estimated or unavailable from the foundry measurements. Thus, the slight difference observed in Fig. 8 is not unexpected.

6. CONCLUSIONS

We present a circuit which generates a quasi-constant current and NTC and PTAT voltages, useful for voltage references and temperature sensors. The circuit needs no resistors, thus it can be fully integrated while keeping a reduced area even for a current under $50nA$ (for $T \leq 370\,K$). We developed a theoretical model which has very good agreement with measurements. This model is based on novel results of the temperature behaviour of some simple circuits when driven by a current with a particular but easily obtained temperature characteristic.

We are currently working on the tradeoff between temperature limits, leakage currents, consumption and area. Future work also includes assessing the effects of noise. This will allow us to obtain a complete, fully integrated, temperature sensor based on this approach.

7. ACKNOWLEDGEMENT

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8. REFERENCES

[1] P. Aguirre and C. Rossi. Architectures and cells for micropower temperature sensors. In *Proc. of the X Workshop Iberchip*, Cartagena de Indias, Colombia, Mar. 2004.

[2] P. E. Allen and D. R. Holberg. *CMOS analog circuit design*, chapter 4. Oxford University Press, New York, USA, 2nd edition, 2002. ISBN 0-19-511644-5.

[3] D. F. Hilbiber. A new semiconductor voltage standard. In *Proc. of the IEEE Int. Solid-State Circuits Conf*, Feb. 1964.

[4] G. C. M. Meijer and J. Verhoeff. An integrated bandgap reference. *IEEE Journal of Solid-State Circuits*, SC-11:403–406, June 1976.

[5] G. C. M. Meijer, G. Wang, and F. Fruett. Temperature sensors and voltage references implemented in CMOS technology. *IEEE Sensors Journal*, 1(3):225–234, Oct. 2001.

[6] H. J. Oguey and D. Aebischer. CMOS current reference without resistance. *IEEE Journal of Solid-State Circuits*, SC-32(7):1132–1135, July 1997.

[7] Y. P. Tsividis and R. W. Ulmer. A CMOS voltage reference. *IEEE Journal of Solid-State Circuits*, 13(6):774–778, Dec. 1978.

[8] E. A. Vittoz and O. Neyroud. A low-voltage CMOS bandgap reference. *IEEE Journal of Solid-State Circuits*, SC-14(3):573–577, June 1979.

[9] R. J. Widlar. New developments in ic voltage regulators. *IEEE Journal of Solid-State Circuits*, SC-6(1):2–7, Feb. 1971.

[10] P. Y. Yu and M. Cardona. *Fundamentals of Semiconductors: Physics and Materials Properties*. Springer, 2nd edition, 1999.