EXPANDING THE URUGUAYAN PUBLIC PACKET NETWORK: NEW ARCHITECTURES FOR THE MAIN SWITCH

Juan Grompone, Member, IEEE
Omar Barreneche, Member, IEEE (*)
Zabala 1378, Montevideo 11000, Uruguay

Abstract - This paper discusses the expansion of the main switch in the Uruguayan public packet network (URUPAC). The switch is an indigenous development based on several prior designs for the telex and data public networks. The advantages of a distributed architecture are presented. The choice of a communication bus was in the past a very difficult item. Several alternatives are discussed according to the expected network growth in the next years (from 64 to 512 communication ports). The best alternative is to use a local network to link concentrators and processors. IEEE 802.3 is a suited protocol. The maximum growing capacity is discussed in this case.

I. INTRODUCTION

Interfase S.A. has developed several switches with stored program control for different telex and data services in the last 13 years [1]. This period begins with a telex switch for 128 terminals. This development was revised in three opportunities; each time the amount of terminals was twofold augmented until a capacity of 1024 terminals was achieved.

With this background experience, a packet switch for 32 data terminals was developed. At present this equipment is being redesigned with the objective of duplicating the quantity of supported terminals (**).

The current growth forecasts for the public data network suggest that the size of the switch will duplicate each year towards a final size of 512 terminals.

The purpose of the present paper is to discuss different alternatives to meet the proposed growth in the next years.

II. DISTRIBUTED ARCHITECTURES

The switches were always built with a distributed architecture. A central processor communicates with several peripheral processors through a communications bus. Figure 1 shows a typical architecture of a telex switch. Figure 2 shows the architecture of the packet data switch for 32 terminals.

(*) Juan Grompone, Director of Telecommunications Division. Omar Barreneche, Head of Hardware Design. Both with Interfase S.A.

(**) All the switches mentioned in the present paper were developed and built for the Administracion Nacional de Telecomunicaciones de Uruguay (the National Telecommunications Administration of Uruguay), and constitute the backbone of the public networks of the country.

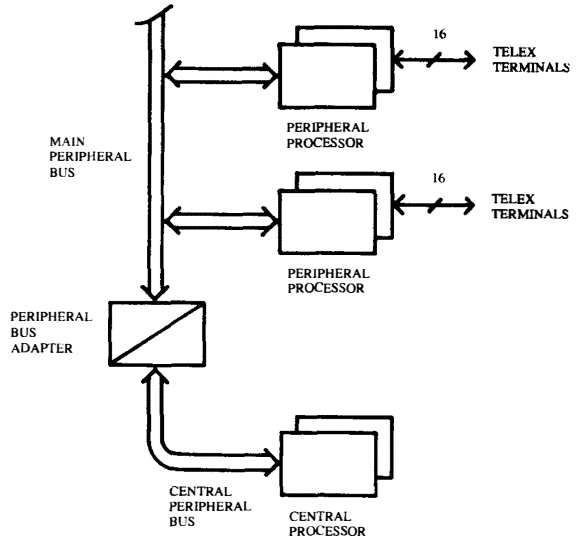

Fig. 1. Architecture of a telex switch. The peripheral bus adapter is the solution to overcome growth demands.

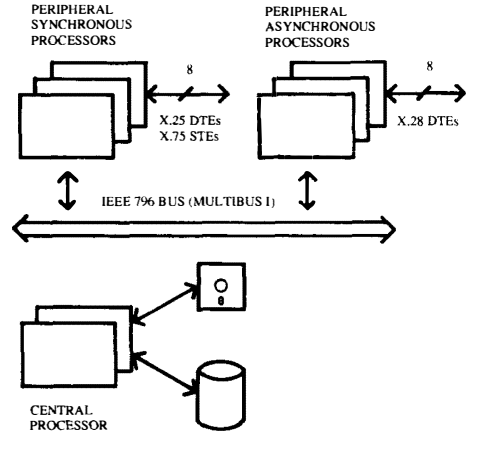

Fig. 2. Architecture of the current packet data switch. A strong-coupled multiprocessor system supporting up to 48 DTEs.

Up to the present, the hardware is based on the IEEE 796 standard (Intel's MULTIBUS I). Standard off the shelf boards are used.

As Figure 1 shows, the central processor and the peripheral processors of the telex switches are MULTIBUS I machines. The communications bus of these switches is a parallel, proprietary bus at 256 KBPS, with two different sections for design reasons. An adapter interfaces the central processor and the peripheral processors sections.

The experience acquired in the successive redesigns shows that the problem of the communications bus is difficult to solve. For compatibility reasons, the peripheral processors section was always kept. In every redesign the adapter and the central processor section of the bus were modified, to support the growth.

As a result of this experience, the packet data switch for 32 terminals was developed as a single MULTIBUS I system, as shown in Figure 2. In this case a standard was adopted to avoid the design and growth flaws that occurred in the telex switches design cycle.

The structure of MULTIBUS I does not allow growing beyond 48 terminals. For the sake of reliability, a peripheral processor takes care at most of 8 terminals in the current design. With this modularity, 64 peripheral processors are at least needed to build a switch for 512 terminals.

For all the above stated reasons, the expansion of the data switch demands a careful analysis of new communication structures. Figures 3 and 4 sketch two architectural proposals with peripheral processors acting as terminals multiplexors. A central processor interconnects these processors.

In Figure 3 a star topology is proposed, with point to point links between the central and the peripheral processors. In Figure 4 a linear topology is proposed, under the principle of the multiple access to the communications medium.

III. COMMUNICATION ALTERNATIVES

The expansion of a 32 terminals switch towards one with 512 terminals strongly suggests a central processor-peripheral processor organization. To maximally reuse the existent design, it is natural that a peripheral processor handles 32 terminals and that the central processor, through the communications bus, performs the routing, switching and management tasks. For compatibility reasons, the peripheral processor should be a MULTIBUS I machine with an architecture similar to the one sketched in Figure 2, excepting that it does not need magnetic media storage.

The remaining design options to discuss are two:

- The structure of the central processor.
- The communication among processors.

The possible alternatives for the central processor structure are few, if compatibility with the precedent design is sought. Like the current version of the switch, it must be a multiprocessor system, with different processors devoted to the link and network layers of the OSI model [2].

Since the costs of a application specific hardware design are impossible to afford, only standard commercial boards come into question. Therefore, the following alternatives are considered:

- Central Processor under MULTIBUS I (IEEE 796).
- Central Processor under MULTIBUS II (IEEE 1296).
- Central Processor under ISA or possibly EISA bus.

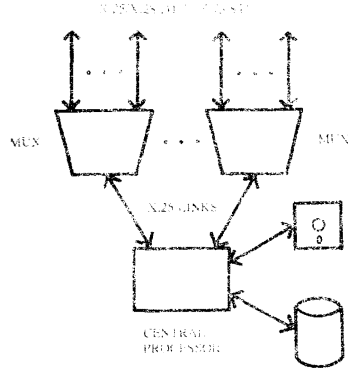

Fig. 3. Proposed distributed architecture of a packet data switch for up to 512 DTEs, with X.25 links between the central processor and the front end multiplexors.

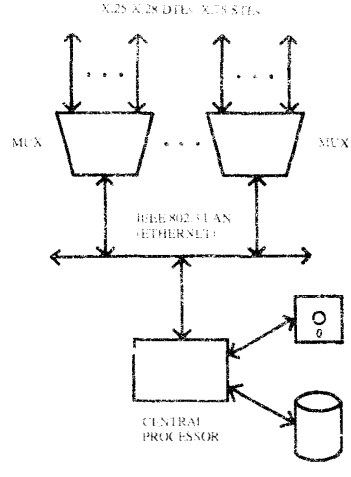

Fig. 4. Proposed distributed architecture of a packet data switch for up to 512 DTEs, with an ETHERNET LAN linking the central processor and the front end multiplexors.

As it has already been noted [3] [4], the switching throughput mainly depends on the central processor. At the current state of the art it is not difficult to achieve a central processor handling a switching capacity of some 1000 packets per second. The experience with the present switch shows that such a capacity suffices for the expansion of the network to 512 terminals. It is also possible to suppose that in a few years processors with a fourfold capacity will be available.

The above stated reasons leaded to the conclusion that the fundamental selection criteria are the maximum amount of peripheral processors a given central processor can handle

and the corresponding costs. These characteristics are strongly dependent on the bus structure and the commercial offer for this bus.

Another equally important aspect in making a selection are the perspectives for the next years of the selected technology, since this is a project that will take about three or four years to be implemented. In this regard it is important to note that at this moment an evolution in the buses standards takes place and it is not certain which one shall predominate. An erroneous bet could drive to extremely high costs in the future, because of incompatibilities.

The communication among processors can take place in three basic alternatives:

-Parallel bus, either standard or proprietary

-Point to point communications, following the X.25 standard [5] at 64 KBPS.

-Multiple access communications, following the IEEE 802.3 (Ethernet) standard [6] [7].

The parallel bus alternative is unattractive. At first, it was impossible to identify a satisfactory standard bus. In case of a proprietary bus, the previous telex experience was a negative one. Table 1 shows a comparison of some of the most relevant characteristics of the remaining alternatives.

The X.25 alternatives have the definite advantage of being already implemented. Its disadvantages are that its point to point nature inherently makes all reconfiguration operations difficult and that every attempt of using redundancy mechanisms to improve reliability steeply raises its costs.

The IEEE 802.3 (Ethernet) alternative has the lack of previous experience of the development team as a disadvantage. In spite of this, its relative cost is not excessive, it enjoys a great flexibility and, because of being a widely accepted open standard, it allows connectivity to a broad spectrum of systems.

An architecture based on this alternative has the additional advantage of permitting more than one central processor to achieve redundancy. In large switches it is mandatory to have at least a duplicated central processor in warm stand-by. This can be easily achieved, since the warm stand-by can permanently monitor the traffic in the communications medium. Moreover, also triple modular redundancy can be implemented, as in the large telex switches. In this case, the peripheral processors act as voters and decisions are taken by majority.

Last but not least, the implementation of the Logical Link Control Sublayer (IEEE 802.2 [8]) opens the way for a future migration to a optical fibers link, if the saturation of the Ethernet link is reached.

The conclusion drawn from this analysis was that the best alternative is evolving towards a IEEE 802.3 based local area network and to leave open the central processor structure. This option results specially attractive since the final objective, the 512 terminals switch, will only be reached after several intermediate redesign stages. In each stage the best cost/performance alternative of the structure will be selected.

IV. MAXIMUM GROWTH

To determine the maximum growth, it is interesting to calculate the packet throughput that can be supported under IEEE 802.3 (Ethernet) communication.

In the local area network, packets flow among the peripheral processors, acting as multiplexors, and the central processor, which is the actual switch. The measurements performed on the present switch show that the mean packet size is 24 bytes. Ethernet frames are 64 bytes long minimum, so this will be the mean size of the frames in the LAN.

COMMUNI-CATION	CENTRAL PROCESSOR BUS	MAXIMUM GROWTH	RELATIVE COST
X.25	IEEE 796	256	MEDIUM
X.25	IEEE 1296	512	HIGH
X.25	ISA/EISA	128	LOW
IEEE 802.3	ALL	>512	VARIABLE

Table 1. Characteristics of some distributed architectures. Maximum growth shows the maximum amount of terminals supported.

The efficiency of an Ethernet based local area network has been extensively studied [3] [9]. For a switch supporting 16 multiplexors with 32 terminals each (512 in the whole), the efficiency of the LAN is about 25%. The effective bit rate in the medium shall be about 2,5 MBPS. This implies a "raw" transfer capacity of

$$\frac{2{,}5 \text{ MBPS}}{64 * 8} = 4900 \text{ packets per second}$$

Taking into account that each packet flows twice, at first from the input multiplexor towards the switch, and then from the switch towards the output multiplexor, the resulting capacity of the channel is the half, that is, about 2400 packets per second.

To determine the throughput capacity after the definition given in CCITT's X.135 Recommendation, it is necessary to analyze the case in which only maximum length data packets flow in the channel. Let us assume that only data packets L bytes long and RR packets (3 bytes long) are transmitted over the LAN. For the data packets, the size of the frames is L + 26 bytes, owing to the protocol overhead, and for the others the size is 64 bytes. The mean size of the frames, considering that there is a one to one correspondence between data and RR packets, is

$$\frac{L + 90}{2}$$

If L = 128 bytes, the mean size of the frames is 109 bytes and the efficiency of the Ethernet LAN for 16 multiplexors is about 40%. As a result, the capacity of the channel is

$$\frac{4 \text{ MBPS}}{109 * 8 * 2} = 2300 \text{ packets per second}$$

If L = 256, the typical frame shall be 173 bytes, the Ethernet LAN efficiency of 60% and the supported capacity shall be

6 MBPS
---------- = 2150 packets per second
173 * 8 * 2

The results shown above indicate then, that the Ethernet LAN allows to reach the expected growth. Its throughput does not limit the central processor and the load increment demanded by the expansion can be met.

V. CONCLUSIONS

The proposed architecture consisting of peripheral processors and a central processor linked by local area network based on the IEEE 802.3 (Ethernet) standard has the following advantages:

-The IEEE 802.3 (Ethernet) standard is well known and spread and most of the systems manufacturers adheres to it. This insures that its incorporation costs shall have a at least constant or, more probably, decreasing costs.

-It offers great flexibility for the reconfiguration of the switch, including dynamic reconfiguration.

-It is an open system, which allows to incorporate most of the new hardware developments.

-It makes possible to add new features to the system, as for example, the engagement of strongly coupled processors as the system's console.

-It allows the use of every kind of redundancy, even at the communications channel level.

According to the previously shown calculations, this architectureshall smoothly adapt itself to the growth of the national data network in Uruguay in the forthcoming years. Furthermore, it allows the reutilization of the hardware and software.

REFERENCES

[1] J. Grompone, "Redes Públicas de Datos: 13 Años de Diseño Nacional", presented at "1er. Simposio de Comunicaciones en el Uruguay", Asociación de Ingenieros del Uruguay / IEEE Uruguay, Montevideo, April 24-28 1989.

[2] O. Barreneche, J. Grompone, and F. Brum, "El Modelo OSI con Arquitectura Multiprocesador", presented at "1er. Simposio de Comunicaciones en el Uruguay", Asociación de Ingenieros del Uruguay/IEEE Uruguay, Montevideo, April 24-28 1989.

[3] J. Nabielsky, "Interfacing to the 10 Mbps Ethernet: Observations and Conclusions", in *Proceedings of the ACM SIGCOMM'84 Symposium, 1984, pp. 124-131.*

[4] O. Barreneche, F. Brum, J. Grompone, and R. Villar, "Ajuste del throughput del Conmutador de URUPAC", in *Anales del 1er. Seminario Estado de la Informática en el Uruguay, 1990, pp. 93-106.*

[5] *CCITT Blue Book, Volume VIII, Fascicle VIII.2, "Data Communication Networks: Services and Facilities, Interfaces"*, Recommendations X.1-X.32, Geneve 1989, pp. 155-314.

[6] *ANSI/IEEE Standard 802.3-1985.*

[7] R. Metcalf and D. Boggs, "Ethernet: Distributed Packet Switching for Local Computer Networks", in *Comm. of ACM*, 19:7 (July 1976), pp. 395-404.

[8] *ANSI/IEEE Standard 802.2-1985.*

[9] A. S. Tanenbaum, "*Computer Networks*", second edition, Prentice Hall, Englewood Cliffs, New Jersey, 1989, pp. 146-148.

[10] *CCITT Blue Book, Volume VIII, Fascicle VIII.3, "Data Communication Networks: Services and Facilities, Interfaces"*, Recommendations X.1-X.32, Geneve 1989, pp. 368-391.

Juan Grompone (M'86) received the Electrical Engineer degree in Engeneering from the School of Engineering of Montevideo, Uruguay, in 1968.

Since 1975 he worked in INTERFASE S.A. From 1975 to 1981 he worked as Design Engineer in Telex Products Department, from 1981 to 1985 as Group Leader of Telex Products Department, and since 1985 as Director of Telecommunications Division.

Since 1986 he worked as Full Proffessor and Head of Department of Computer System Architecture of the School of Engine ering, Montevideo, Uruguay. His research area is Software Engineering and Data Communica tions Systems.

Omar Barreneche (M'88) received the Electrical Engineer degree in Engineering from the School of Engineering of Santiago de Cuba, Cuba, in 1982. In 1986 he joined INTERFASE S.A. where he currently heads the Hardware Design Department. Since 1987 he is Adjunct Professor of the Department of Electronics of the School of Engineering, Montevideo, Uruguay. His research interests are Digital Systems, Real Time Systems, and Data Communications Systems.