DESIGN OF A MICROPOWER SIGNAL CONDITIONING CIRCUIT FOR A PIEZORESISTIVE ACCELERATION SENSOR

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ABSTRACT

The design and test of a micropower signal conditioning circuit for a piezoresistive accelerometer is presented. The circuit is intended for sensing human body motion in rate-adaptive cardiac pacemakers. A strategy is proposed to allow to handle the piezoresistive sensor with the desired level of consumption. Experimental results show the fabricated circuit is able to measure accelerations in the range from 0.04g to 0.34g with a total consumption of less than 3μ A with supply voltages down to 2V.

1. INTRODUCTION

The present work describes the design and test of a micropower integrated circuit to measure accelerations of the human body motion. This circuit is intended to be employed in the construction of rate-adaptive cardiac pacemakers (a pacemaker which varies its stimulation rate according to patient's requirement). This work is included in the project between the Microelectronics Group, Universidad de la República, Montevideo, Uruguay and the Centro de Construcción de Cardioestimuladores del Uruguay (C.C.C.U.), and it is a first approach to incorporate to the pacemaker integrated circuit (now in develop stages at the Microelectronics *Group*) a human activity sensing function.

Three kinds of acceleration sensors have been successfully employed in rate-adaptive cardiac

pacemakers These are piezoelectric, [1]. piezoresistive and capacitive sensors. In this work, a piezoresistive sensor was used due to its low cost compared to the other ones. Despite this benefit, its resistive nature and its resistance value, usually in the K Ω range [1][2], make difficult its application in a micropower In the following sections a environment. technique to overcome this limitation is presented.

The paper is organized as follows: the next section presents the initial specifications of the circuit and its architecture. Section III describes the measurement results and final circuit specifications. Finally in Section IV the main conclusions of this work are summarized.

2. CIRCUIT SPECIFICATIONS AND ARCHITECTURE

The primary specifications for the circuit were the following :

- The circuit must process the signal from a piezoresistive acceleration sensor to give, as an output, a voltage which values correspond to the average of the absolute values of the patient's acceleration in three seconds.
- The accelerations to be measured are in the range from 0.007g to 0.34g with a bandwidth of interest from 0.5Hz to 7Hz. In the case of

the maximum acceleration value, the circuit output should be at least 0.5V.

• Circuit power consumption must be less than $3\mu A$ and it must be able to operate correctly for power supply voltages varying from 2 to 2.8V.

The target process is a standard 2.4µm analog CMOS process with double poly and double metal. This process is intended for 5V supply voltage and has a nominal threshold voltage of 0.85V with a maximum and a minimum of 1.0V and 0.7V respectively. The fulfillment of the requirements in such a process, instead of a lowvoltage specialized process with lower threshold voltages, enables a broader and cheaper range of possible foundries. target processes and However, to work with 2V supply voltage in such a process, various challenges must be overcome.

To reach the requirement of consumption, the strategy applied was based on turning on the sensor only during short time intervals necessary to sample and hold its differential output and then process in continuous time the sampled and held signal. In this way the sensor is only turned on with a very small duty cycle, drastically decreasing its consumption. Figure 1 shows the circuit block diagram.



Figure 1. Block diagram of the conditioning circuit.

In this architecture, the sampled signal is reconstructed by a band-pass filter and amplifier and then the absolute value is taken by a rectifier stage. Finally there is a stage that approximates the three seconds average. We will now describe the structure of the circuit blocks.

The structure found to be suitable for the bandpass filter is the one shown in Figure 2, which is an adaptation of the architecture proposed in [3]. The circuit of Figure 2 implements an instrumentation amplifier with a low pass characteristic, followed by a second gain stage. This gain stages are fedback with an integrator. This feedback loop gives the high pass characteristic of the filter.



Figure 2. Structure of the band-pass filter-amplifier.

For the rectifier stage, several architectures were studied. The standard CMOS n-well technology under which we fabricated our circuit only gives the possibility of using p-n diodes with one terminal connected to the bulk. Therefore, the idea of using diodes was abandoned. Instead, the technique for rectifying was based on the utilization switches of to change the configuration of an amplifier circuit (from inverter to non-inverter and vice-versa) according with the sign of the input signal. At the same time, it is worthy to implement this technique with a continuous time circuit since its input is a reconstructed signal. The resulting circuit is shown in Figure 3.



Figure 3. Continuous time rectifier

Finally, the three seconds averaging stage was approximated by an external passive RC low pass filter.

The design was done under a *top-down* scheme, analyzing in first instance the convenience of the different proposed architectures to finally reach to the dimensions of each transistor involved. This last topic was carried out through the unified treatment of the operation of the MOS transistor in all regions given by the EKV model [4] and through the utilization of the g_m/I_D curve [5]. This approach allowed to optimize the consumption of the circuits by working in weak and moderate inversion when needed.

A model and methodology for evaluation of the effects of the switch on-resistance and leakage currents in the transfer function of the sample and hold in this application were developed and reported in reference [6].

Figure 4 shows a microphotograph of the circuit.



Figure 4. Microphotograph of the circuit.

3. EXPERIMENTAL RESULTS AND CIRCUIT SPECIFICATIONS

Two kind of electrical tests (each one carried out for 2V and 2.8V) were done for evaluating the performance. The first one included an exhaustive test of each building block that gave results in accordance with what it was expected. The second test characterized the overall performance of the circuit. The results obtained in these tests showed that all primary requirements were accomplished excepting the one concerning to the minimum distinguishable acceleration (0.007g). The minimum measured value resulted to be 0.04g, which is satisfactory for biomedical purposes. This difference is due to "thermal and flicker noise" of the band-pass filter, which are very important when dealing with low signal amplitudes and low frequencies.

Another aspect to be improved is the following: the limited input range allowed at the feedback input of the instrumentation amplifier, where the output of the integrator is connected to (see Figure 2), made that the DC input values that are acceptable are limited. This led to malfunction in a few high offset prototypes among the tested ones. An alternative design of the instrumentation amplifier that solves this problem is currently being fabricated. The main measured specifications of the circuit are summarized in the following table:

| | Min. | Тур. | Max. |
|---|---------------------------------|---------------|-------------------------------|
| Amplifier | 2900 | - | - |
| Gain | | | |
| Equivalent | - | 18 | - |
| input noise | | | |
| (µVrms) | | | |
| Consumption | n 2.5 | - | 3 |
| (µA) | | | |
| Area (mm ²) | - | 1.82 | - |
| 200 ppm 180 ppm 160 - 140 - 120 - 100 - 80 - 40 - 20 - 0 - | Simulated heart Real rate | rate heart | Activity level how time |
| -20 🗄 | 50 | 100 | 150 20 |

Figure 5. Overall "field" performance.

Finally some initial "field" tests were done. The results of one of this tests are shown in Figure 5 where the heart rate of a healthy person doing physical exercise is compared with the simulated heart rate generated by the pacemaker algorithm, fed with the digitized output of the circuit developed in this work, shown in the bottom curve of Figure 5 ("activity level"). The test consisted of different levels of physical activities like walking and running.

4. CONCLUSIONS

As a conclusion, we can mention that a micropower signal conditioning circuit for a piezoresistive acceleration sensor, suitable for low supply voltages, was proposed, designed and tested. A strategy consisting of turning on and off the sensor to sample its signal to reduce consumption was studied and designed, allowing to implement a signal conditioning circuit with a total consumption of less than $3\mu A$. The design of the circuit architecture managed to solve the problems related, on one hand, to the application of a standard (no low voltage technology) at 2V power supply and, on the other hand, to the low input signal levels (minimum amplitude of $23\mu Vrms$).

5. **REFERENCES**

- [1]J. Webster, *Design of Cardiac Pacemakers*, IEEE Press, Piscataway, NJ, 1995.
- [2]ICSensors, Accel. 3022 and 3028:OEM Accelerometer Piezoresistive Low Cost, Data Sheet.
- [3] M. Steyaert, W. Sansen, C. Zhongyuan, "A micropower low-noise monolithic instrumentation amplifier for medical purposes", *IEEE Journal of Solid-State Circuits*, vol. SC-22, no. 6, pp. 1163-1168, Dec. 1987.
- [4] C. Enz, F. K. Krummenacher and E. A. Vittoz, "An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications", Analog Integrated Circuits and Signal Processing, No.8, pp. 83-114, 1995.
- [5] F. Silveira, D. Flandre, P. G. A. Jespers, "A g_m/I_D Based Methodology for the Design of CMOS Analog Circuits and Its Application to the Synthesis of a Silicon-on-Insulator Micropower OTA", *IEEE Journal of Solid State Circuits*, Vol. 31, No.9, pp. 1314-1319, Sep. 1996.
- [6] A. Arnaud, F. Silveira, "The design methodology of a sample and hold for a low power sensor interface circuit", *Proceedings* of the X Brazilian Symposium on Integrated Circuit Design, Gramado, Brazil, August 1997, pp. 243-252.