A 2V Rail-to-Rail Micropower CMOS Comparator.

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Abstract

The design of a rail-to-rail micropower comparator in CMOS technology is described. The circuit is intended for implantable biomedical devices powered by batteries, with a total consumption of 500nA and operation up to supply voltages of 2V. This cell, currently being fabricated, has a core die area of 0.27 mm^2 on a 2.4###m standard analog CMOS technology with a 0.85V nominal threshold voltage. It is expected to have a typical response time of 35µs ###and an offset voltage of about 6mV. The limitations imposed by the low supply voltage are presented. The ways of overcoming these limitations, based on an accurate sizing of the transistors for operation in the weak and moderate inversion regions are studied. An approach, based on a capacitive D/A converter, for the generation of a comparison reference input that is digitally programmable is also presented.

I. Introduction.

The presented design provides a combination of a rail-to-rail comparator and a digitally programmable reference level generation circuit. It was designed to fit the requirements for processing cardiac signals in implantable cardiac assist devices. Its goal is to detect signals which amplitude exceeds a programmable threshold. Coupled with a successive approximation register function it may also be used to implement a successive approximation A/D converter. In Section II we introduce the characteristics of the signals to be processed and the constraints and initial specifications imposed by the field of application. Section III discusses the reasons that lead to the chosen circuit topology. Special consideration is directed to the limitations associated with the low supply voltage requirement. Section IV presents the design methodology. Finally Section V shows the simulation results[1] and in Section VI the conclusions are summarized.

II. Characteristics of the Input Signal and Specifications.

The input signals of the circuit are cardiac signals previously filtered and amplified. A standard test waveform representing the cardiac signal is a triangular wave with 2ms rise time and 13ms fall time, sometimes referred as "Tokyo signal" [1]. This signal was applied throughout the circuit development to characterize performance aspects that may depend on the input waveform like the comparator delay. Neither this slow varying input signal nor the low-speed digital circuit that will process the output of the comparator in the final application are much demanding on the speed of the comparator. The initial specification for the comparator maximum delay was set at 0.5ms.

The offset voltage specification derives from the minimum amplitude of the amplified cardiac signal that the comparator must handle that is 62.5mV. To have a maximum desired error of 10% in the amplitude detection, the offset voltage must be lower than 6.25mV.

The remaining specifications are associated to the incorporation of this cell to a battery operated implantable device. The full charge voltage of a Lithium-Iodine battery applied in these devices is 2.8V and the circuit must be fully operative for supply voltages up to 2.0V to guarantee operation during an acceptable lapse of time from the detection of the battery low condition to the replacement. Therefore the circuit was synthesized for 2V supply voltage. The target current consumption was set at 500nA.

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[1] The circuit is being fabricated at the time of submission of this paper. We expect to be able to show experimental results during the conference.

Finally, the global architecture of the circuit where this comparator will be applied requires to handle rail-to-rail input signals.

The target process is a standard 2.4μm### analog CMOS process with double poly and double metal. This process is intended for 5V power supply and has nominal threshold voltages of nMOS (pMOS) transistors of 0.85V (-0.85V) with a minimum and maximum specified values of, respectively, 0.7V (-0.7V) and 1.0V (-1.0V). The fulfillment of the requirements in such a process, instead of a low-voltage specialized process with lower threshold voltages, enables a broader and cheaper range of possible target processes and foundries. However, the rail-to-rail operation with 2V power supply in such a process presents various challenges that are presented in the next section as well as the means we propose to overcome them.

III. Selection of the Circuit Topology. Low Voltage Design Issues.

The factors that determined the circuit topology were the 2V supply voltage, the rail-to-rail input operation requirement and the very low supply current available.

The first important limitation set by the first two referred factors is to preclude the utilization of switches to handle the input signal unless a on-chip clock-voltage multiplication scheme is applied. We decided to try to avoid the clock-voltage multiplication alternative for simplicity and reliability reasons. The limitation on the application of switches is illustrated in Fig. 1 that plots the on conductance and on resistance of a switch, implemented as the parallel connection of a n and pMOS transistors driven by complementary signals, as a function of the input voltage to the switch. The EKV model ([2,3]), that gives a representation valid in all regions of operation, was applied for the transistors. Fig. 1 shows that exists a gap in the input voltage range where both the transistors are virtually cut off and the on resistance is excessively high, even for the low speed application under consideration where a relatively high RC time constant would be acceptable. To decrease the on resistance to acceptable levels by increasing the aspect ratio of the transistors is also non practical because it would lead to a unacceptable charge injection error.

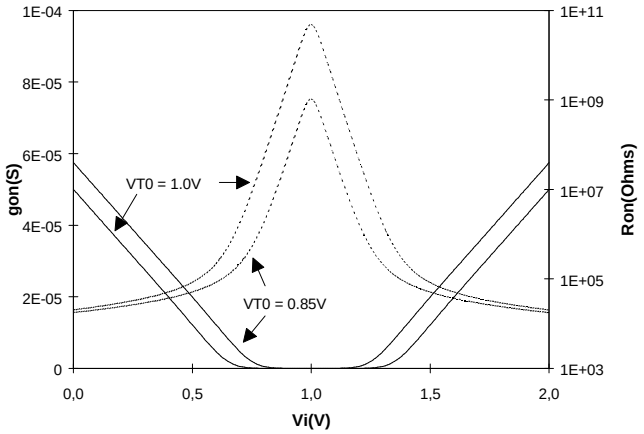

Fig 1. On conductance (solid lines) and resistance (dashed lines) of CMOS switch vs. input voltage for 2V power supply with nominal threshold voltage (V_{T0} = 0.85V) and maximum threshold voltage (V_{T0} = 1.0V).

We can classify comparator topologies according to their principle of operation in 3 broad classes [4,5,6]: (i) based on a high gain amplifier, (ii) regenerative or positive feedback based and (iii) other switched capacitor based architectures. Let's briefly describe each of these alternatives and evaluate them to the light of the above requirements. Topology (i) is typically an open loop op-amp without internal compensation, sometimes in a multistage configuration to increase the speed. The second class of topology takes advantage of the positive feedback of a flip flop like structure to speed up the comparison. Although exceptions exists [4], these circuits usually apply one of the following principles: 1) a switch equals both outputs of the flip-flop forcing it to its state of unstable equilibrium and then lets it to evolve to the final state according to the difference between the comparators inputs, or 2) with the flip flop structure turned off, a couple of switches force the outputs to be equal to the comparator inputs (or their amplified version) and then turns on the flip flop that will evolve to the final state. Therefore this structure is discarded because it requires a switch operating in the whole power supply range. The topologies corresponding to the third class as well as the switched capacitor techniques available to cancel out the comparator offset cannot be applied for the same reason.

Therefore an op-amp based comparator topology was chosen. The input stage of the op-amp was determined by the rail-to-rail input requirement. The parallel combination of a n and a p differential pair was

selected [7, 8]. As will be shown in the next section, the low speed required as well the high gain achievable operating in weak inversion allow the application of a single stage structure. Therefore the amplifier topology shown in Fig. 2 was considered. It is an adaptation of the well known "symmetrical OTA" ([9]) structure to the rail-to-rail input stage.

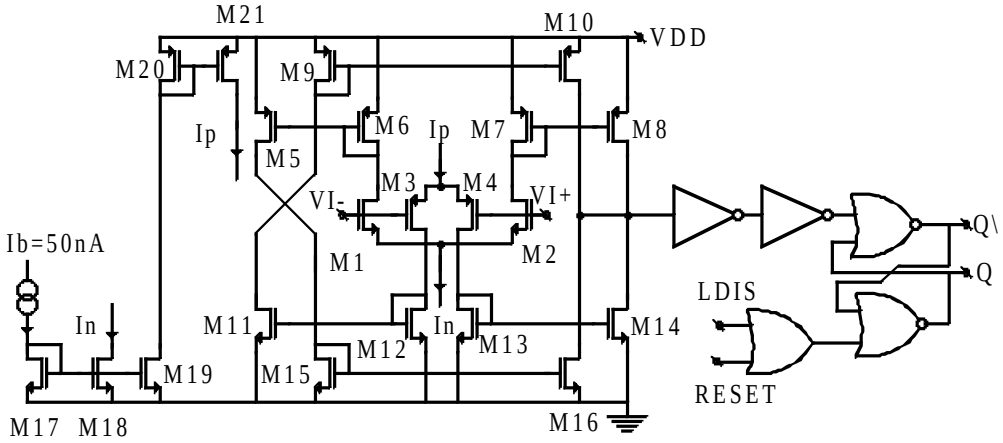

Fig. 2: Comparator schematic diagram.

Following the amplifying stage a minimum sized buffer (to minimize the amplifier load capacitance) and a latch are included. The latch may be also set to transparent mode to have a non-latched output.

To guarantee the rail-to-rail input operation the following condition must be fulfilled:

$$V_{DD} \geq V_{GSp} + V_{GSn} + 2.V_{DSAT} \quad (1)$$

where V_{DD} is the supply voltage, V_{GSp} and V_{GSn} are the gate source voltage of the p and n input pair transistors and V_{DSAT} is the minimum voltage required across the transistors of the current sources at the source of the differential pairs (M18 and M21) to ensure they are saturated and operate as a current source. This condition ensures that the regions of operation of the n and p differential pairs overlap near $V_{DD}/2$ and does not exists a gap where none of the pairs work.

It seems difficult to satisfy condition (1) for V_{DD} = 2V and the nominal V_{T0} of 0.85, moreover for the worst case condition of V_{T0} eqaul to 1.0V. However the low V_{GS} values reached when operating in moderate and weak inversion in the subthreshold region, together with the low saturation voltages allow to satisfy condition (1) even for V_{T0} of 1.0V. The next section describes the methodology followed to size the transistors to achieve the performance desired and to satisfy condition (1).

A digitally programmable reference level generation circuitry compatible with the low power consumption required, was implemented based on the charge redistribution D/A converter principle ([10]). It's schematic diagram is shown in Fig. 3. It's worth to note that in this structure all the switches are connected either to ground or to the power supply, hence do not have the problem referred above.

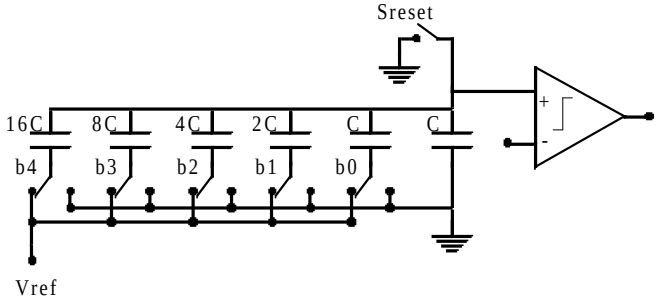

Fig. 3. Digitally programmable comparison level generation circuit.

IV. Design methodology.

The sizing of the transistors was done through the method presented in [11,12]. This method, that is based on the relation between the transconductance over drain current ratio (g_m/I_D) and the normalized current $I_D/(W/L)$, allows a unified treatment of all regions of operation of the MOS transistors. The application of this

method coupled with the EKV model with a set of parameters extracted from measurements for the target process, allows an accurate sizing of the transistors.

The synthesis procedure followed was:

1. From the total consumption specification and the circuit topology of Fig. 2 the current through each transistor was determined.

2. A g_m/I_D value is chosen for each transistor. From this value, proceeding as explained in [11, 12], a $I_D/(W/L)$ value is obtained from the g_m/I_D vs. $I_D/(W/L)$ relation and then using the I_D value deduced in 1, (W/L) is obtained. The selection of g_m/I_D is based on different trade-offs depending on the considered transistor. Let's illustrate the approach with the case of the input differential pairs and of the current sources of the differential pairs.

2.a For the input differential pairs a higher value of g_m/I_D will give, on one hand, higher g_m (and hence speed) for a given I_D, higher gain, lower gate-source, saturation and offset voltages; on the other hand a higher g_m/I_D requires lower values of $I_D/(W/L)$ and therefore bigger transistors and parasitics for a given current. Moreover, due to the flat characteristic of the g_m/I_D vs. $I_D/(W/L)$ curve near the weak inversion region, in this region a small increment of g_m/I_D requires a big increment of (W/L). By exploring the design space through the g_m/I_D method we can choose the best compromise between performance and area. This approach lead to a value of g_m/I_D = 24 for the input differential pairs transistors that corresponds to (W/L) of 29 for the nMOS transistors and 69.5 for the pMOS transistors. The corresponding V_{GS} value for this transistors sizes is 0.7V for V_{T0}=0.85V and 0.85V for V_{T0}=1V. This values of V_{GS} are compatible with condition (1) with a 2V power supply and V_{DSAT} corresponding to operation near weak inversion of about 0.15V. It's interesting to note that a g_m/I_D value of 25 (fully in the weak inversion region) leads to (W/L) values of 198 and 477 for the n and p transistor respectively, offering a negligible increase in gain or speed and V_{GS} at V_{T0} equal to 1.0V is only reduced from 0.85V to 0.77V.

2.b A higher g_m/I_D of the current mirror transistors implementing the current sources of the differential pair is reflected on a lower saturation voltage, but on poorer noise and matching properties and higher (W/L) values, that in the case of a current source is critical because non minimum length transistors are used to increase the output impedance.
The chosen value of 22 corresponds to (W/L) equal to 25 for the p transistors and 10.4 for the n transistors. This value allows an acceptable behavior of the current source with V_{DSAT} of 0.15V while the estimated rms noise current (0.24nA) is negligible with respect to the bias current of 100nA.

3. A L value is chosen for each transistor. For the differential pair transistors minimum length can be chosen. In our case a non minimum value was chosen based on reliability considerations. For the current mirrors, the L value is derived from a trade-off between its influence on the current mirrors output impedance (and through it on the amplifier gain and common mode rejection ratio) and on the transistors size and parasitics that influence the circuit speed.

4. The gain, speed and offset are predicted and checked against the desired performances. If they are not acceptable, the chosen g_m/I_D, L values or current consumption specification must be modified.

The resulting transistors sizes are shown in Table 1. In the considered process the final sizes are derived from the drawn sizes after a 0.8 factor shrink. The dimensions indicated below are drawn dimensions.

Transistor	W/L (###m)	g_m/I_D	Transistor	W/L (###m)	g_m/I_D
M1,2	278/4	24	M17,M19	62.5/12	22
M2,3	116/4	24	M18	125/12	22
M5-10	50/24	18	M20	150/12	22
M11-16	21/24	18	M21	300/12	22

Table 1. Transistors dimensions. All dimensions are drawn dimensions that are shrunk by a 0.8 factor before fabrication.

Fig. 4 shows the layout of the comparator cell and of the complete chip including the reference generation circuitry.

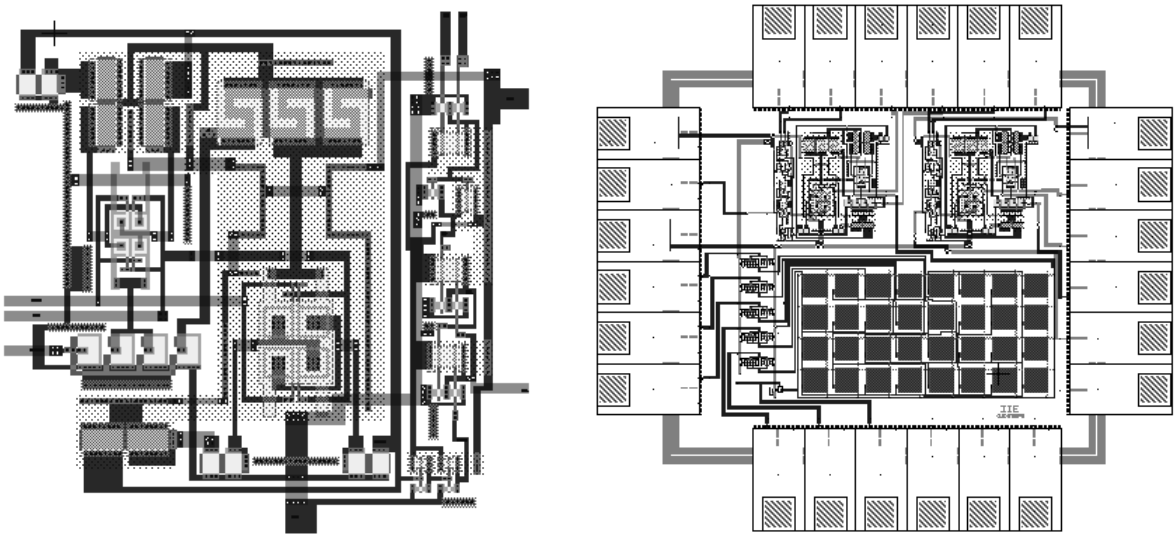

Fig. 4 Layout of comparator cell and complete chip.

V. Expected performances.

The main circuit characteristics are summarized on Table 2.

Supply Voltage	2 V	
Total Standby Current	500 nA	
Typical Delay	35 ###s	100mV input step with 5mV overdrive, Common mode range: 0.2V - 1.8V.
Maximum Delay	170 ### s	32.5mV input triangular signal with 1.5mV overdrive, Common mode range: 0.2V - 1.8V.
Amplifier gain	59 dB	Common mode level: 0.3V
Amplifier gain	61 dB	Common mode level: 1.0V
Amplifier transition frequency	235 kHz	Common mode level: 0.3V, Load Capacitance: 0.42pF
Amplifier transition frequency	344 kHz	Common mode level: 1.0V, Load Capacitance: 0.42pF
Offset voltage	6.6 mV	Estimated with representative matching data from Refs. [13] and [14]: β standard deviation $\sigma\beta$=0.2% and V_{T0} standard deviation σ_T=2mV.

Table 2. Circuit characteristics.

Fig. 5 shows a simulation of the circuit using the EKV model where the rail-to-rail operation of the circuit can be appreciated.

VI. Conclusions.

The presented design is compatible with the requirements for processing cardiac signals in implantable devices operating from 2V battery voltage with a total consumption of 500nA. The limitations imposed by the low supply voltage were discussed. The method followed to precisely size the transistors to operate in the weak and moderate inversion regions was presented. This approach allowed to lower the gate-source and saturation voltages, achieving rail-to-rail input operation even in the worst case condition of 1.0V maximum threshold voltage.

Acknowledgments: The authors wish to thank the Centro de Construcción de Cardioestimuladores del Uruguay S.A. and its technical staff for their support of this work.

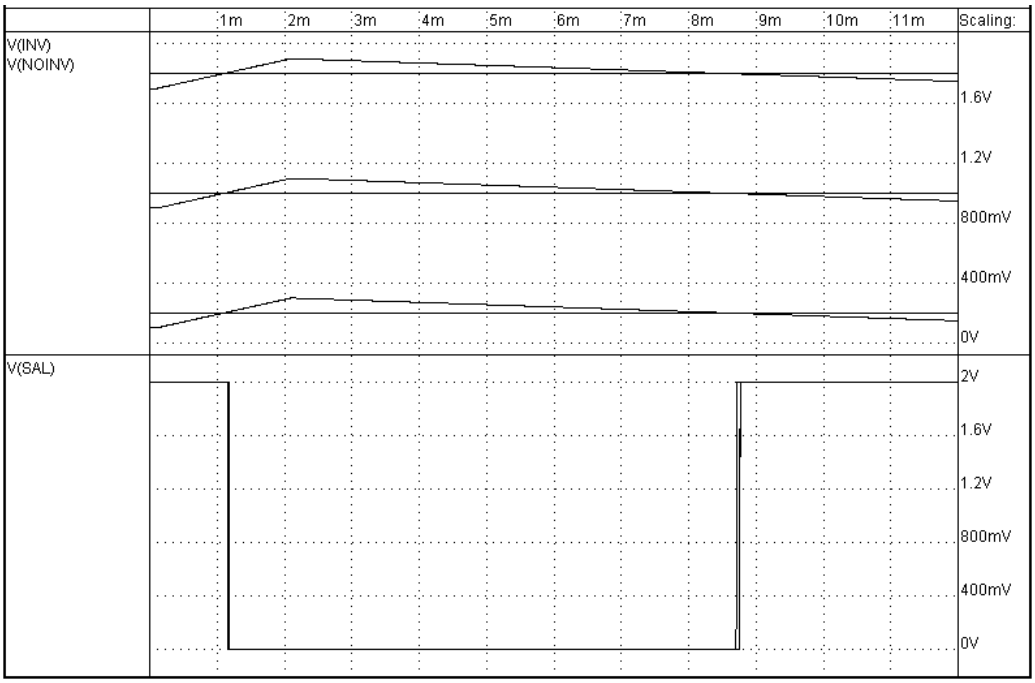

Fig. 5 Simulation results. Top window: comparator inputs, bottom window: comparator output.

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