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Current efficient integrated architecture for common mode rejection sensitive neural recordings

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To Fiorella, Valentina, Camila, and Graciela.

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Abstract

In the last decade we have seen a significant growth of research and potential applications of electronic circuits that interact with the nervous system, in a wide range of applications, from basic neuroscience research to medical clinic, or from the entertainment industry to transport services. The real time acquisition and analysis of brain signals, either through wearable electroencephalography (EEG) or invasive or implantable recordings, in order to perform actions (brain machine interface) or to understand aspects of brain operation, has become scientifically and technologically feasible.

This thesis aims to support neural recording applications with low noise, current-efficiency and high common-mode rejection ratio (CMRR) as main features of the recording system. One emblematic example of these applications in the neuroscience domain is the weakly electric fish neural activity recording, where the interference produced by the discharge of the fish electric organ is a key factor. Another example, from the implantable devices domain, is the nerve activity recorded with cuff electrodes, where the desired signal is interfered by electromyographic potentials generated by muscles near the cuff. In these cases, the amplitude of the interfering signals, which mainly appear in common mode, is several orders of magnitude higher than the amplitude of the signals of interest.

Therefore, this thesis introduces a novel integrated neural preamplifier architecture targeting CMRR sensitive neural recording applications. The architecture is presented and analyzed in depth, deriving the preamplifier transfer function and the main design equations. We present a detailed analysis of a technique for blocking the input dc component and setting the high-pass frequency without using MOS pseudo-resistors. One of the main contributions of this work is the overall architecture coupled with an efficient and simple single-stage circuit for the preamplifier main transconductor. A fully-integrated neural preamplifier, which performs well in line with the state-of-the-art of the field while providing enhanced CMRR performance, was fabricated in a 0.5 μm CMOS process. Results from measurements show that the measured gain is 49.5 dB, bandwidth ranges from 13 Hz to 9.8 kHz, CMRR is very high (greater than 87 dB), and it is achieved jointly with a remarkable low noise (1.88 μV_{rms}) and current-efficiency (NEF = noise efficiency factor = 2.1). A second version of the preamplifier with one external capacitor achieves a high-pass frequency of 0.1 Hz while keeping the performance of the fully-integrated version.

In addition, we present in-vivo measurements made with the proposed architecture in a weakly electric fish (*Gymnotus omarorum*), showing the ability of the preamplifier to acquire neural signals from high amplitude common mode interference in an unshielded environment. This was the first in-vivo testing of a neural recording integrated circuit designed in Uruguay done in a local lab. Furthermore, signals recorded with our unshielded low-power battery-powered preamplifier perfectly match with those of a shielded commercially-available amplifier (ac-plugged, without power restrictions). To

the best of our knowledge, the proposed preamplifier is the best option for applications that simultaneously need low noise, high CMRR and current-efficiency.

Furthermore, in this thesis we applied the aforementioned architecture to band-pass biquad filters, specially but not only, to those with differential input. The new architecture provides a significant reduction in consumption (up to 30%) and/or makes it possible to block a higher level of dc at the input (up to the double, without using decoupling capacitors).

Next, we applied the novel architecture to the design of the different stages of an integrated programmable analog front-end. Results from simulations shows that the gain is programmable between 57 dB and 99 dB, the low-pass frequency is programmable between 116 Hz and 5.2 kHz, the maximum power consumption is 11.2 μA and the maximum equivalent input-referred noise voltage is 1.87 μV_{rms}. The comparison between our front-end and other works in the state-of-the-art shows that our front-end presents the best results in terms of CMRR and noise, has the greatest value of gain and equals the best NEF reported.

Finally, some system-level topics were addressed during this thesis, including the design and implementation of three prototypes of end-to-end wireless biopotentials recording systems based on off-the-shelf components.

Developing and applying circuits, systems and methods, for synchronized large-scale monitoring of neural activity, sensory images, and behavior, would produce a dynamic picture of the brain function, which is essential for understanding the brain in action. In this context, we hope that the present thesis become our first step to further contribute to this area.

Resumen

En la última década se registra a nivel mundial un crecimiento importante de las investigaciones y potenciales aplicaciones de circuitos que interactúan con el sistema nervioso, en un amplio rango de aplicaciones, desde investigación básica en neurociencia hasta la clínica médica, o desde la industria del entretenimiento hasta servicios de transporte. La adquisición en tiempo real y el análisis de señales del cerebro, ya sea mediante electroencefalografía (EEG) "vestible", registros invasivos o implantados, para realizar acciones (interfaz cerebro máquina), o entender aspectos del funcionamiento del cerebro, se ha vuelto científica y tecnológicamente posible.

Esta tesis tiene como objetivo darle soporte a aplicaciones basadas en el registro de señales neurales donde el bajo ruido, la eficiencia en términos de consumo de corriente y tener una alta relación de rechazo al modo común (CMRR por sus siglas en inglés) son las características más importantes del sistema de adquisición. Un ejemplo emblemático de estas aplicaciones, dentro del mundo de la neurociencia, es el registro de la actividad neural del pez eléctrico, donde la interferencia producida por la descarga del órgano eléctrico del pez es un factor determinante. Otro ejemplo, a nivel de dispositivos implantables, es el registro de la actividad de un nervio mediante electrodos de tipo "cuff", donde la señal de interés es interferida por potenciales electromiográficos generados por músculos cercanos al electrodo. En estos casos, la amplitud de las señales que interfieren, que esencialmente aparecen en modo común, es varios órdenes de magnitud mayor que la amplitud de las señales de interés.

Por lo tanto, esta tesis propone una novedosa arquitectura para preamplificadores neurales integrados orientados a aplicaciones de registro de señales neurales sensibles al CMRR. La arquitectura es presentada y analizada en profundidad, derivando la función de transferencia del preamplificador y las principales ecuaciones de diseño. Además, se presenta el análisis detallado de una técnica para bloquear la componente de continua de la entrada y fijar la frecuencia corte inferior sin utilizar pseudo-resistores MOS. La arquitectura en su conjunto, junto con un circuito sencillo y eficiente para el transconductor principal del preamplificador son una de las principales contribuciones de la presente tesis. Un preamplificador neural totalmente integrado, fabricado en un proceso CMOS de 0.5 μm permite alcanzar el estado del arte con una destacada performance en CMRR. Resultados provenientes de medidas muestran que el CMRR medido es muy alto (mayor a 87 dB), y es alcanzado conjuntamente con un destacable bajo ruido (1.88 μV_{rms}) y eficiencia en términos de consumo de corriente (NEF = noise efficiency factor = 2.1). Una segunda versión del preamplificador utilizando un solo condensador externo alcanza una frecuencia de corte inferior de 0.1 Hz manteniendo la performance de la versión totalmente integrada. Asimismo, se presentan medidas in-vivo realizadas con la arquitectura propuesta en un pez eléctrico (*Gymnotus omarorum*), mostrando la habilidad del amplificador de adquirir, sin blindaje, pequeñas señales neurales superpuestas a grandes interferencias en modo común. Esto constituye la primera vez que se realiza en Uruguay el test in-vivo de un ampli-

ficador neural integrado diseñado localmente. Además, las señales registradas con nuestro preamplificador de bajo consumo (alimentado con baterías y sin blindaje) se corresponden perfectamente con las que registró un amplificador comercial (sin restricciones de consumo y blindado). Hasta donde sabemos, el preamplificador propuesto es la mejor opción para aplicaciones que necesitan bajo ruido, alto CMRR y eficiencia en términos de consumo de corriente.

En esta tesis se extendió y aplicó en filtros bicuadráticos pasa-banda la arquitectura previamente desarrollada, especialmente, pero no solamente, para aquellos con entrada diferencial. La nueva arquitectura ofrece una reducción significativa del consumo (hasta el 30%) y/o hace posible el bloqueo de mayores niveles de continua en la entrada (hasta el doble) sin usar capacitores de desacople.

Asimismo, se aplicó la novedosa arquitectura al diseño de las diferentes etapas de un front-end analógico, integrado y programable. La ganancia se puede programar entre 57 dB y 99 dB, y la frecuencia de corte superior entre 116 Hz y 5.2 kHz. El máximo consumo es 11.2 μA y el máximo ruido equivalente a la entrada es 1.87 μV_{rms}. La comparación entre nuestro front-end y otros trabajos similares en el estado del arte muestra que nuestro diseño presenta los mejores resultados en términos de ruido y CMRR, tiene el mayor valor de ganancia, igualando los mejores valores de NEF reportados.

Finalmente, la tesis plantea algunos tópicos a nivel sistema, incluyendo el diseño y la implementación de tres prototipos "punta a punta" de sistemas de adquisición de biopotenciales basados en componentes estándar.

El desarrollo y la aplicación de circuitos, sistemas y métodos para monitorear actividad neural en forma sincronizada con imagenes sensoriales y comportamiento, podría producir una imagen dinámica de las funciones cerebrales, que es esencial para entender el cerebro en funcionamiento. En este contexto, esperamos que la presente tesis sea nuestro primer paso para continuar contribuyendo en esta área.

Glossary

ADC	Analog to Digital Converter
AFE	Analog Front End
BLE	Bluetooth Low Energy
bps	bits per second
BMI	Brain Machine Interface
BR	Bluetooth Basic Rate
BSN	Body Sensor Network
BT	Bluetooth
CR	Compression Ratio
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Radio
CTPS	Compression Time Per Scalar Sample
DDA	Differential Difference Amplifier
DMA	Direct Memory Access
ECG	Electrocardiogram
EEG	Electroencephalography / Electroencephalogram
EDR	Bluetooth Enhanced Rate
EMG	Electromyographic / Electromyogram
EOD	Electric Organ Discharge
FFT	Fast Fourier Transform
FLO	C implementation of the algorithm proposed in [1]
IC	Integrated Circuit
ICMR	Input Common Mode Range
ISR	Interrupt Service Routine
GUI	Graphic User Interface
kB	kilo byte
kbps	kilo-bits per second
ksps	kilo-samples per second
LFP	Local Field Potential
LNA	Low Noise Amplifier
Mbps	Mega-bits per second
MC	Monte Carlo
MCF	Multi-Channel Fixed Compression Algorithm

MCS	Multi-Channel Speck Compression Algorithm
MCU	Microcontroller Unit
NEF	Noise Efficiency Factor
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PEF	Power Efficiency Factor
PSRR	Power Supply Rejection Radio
RLS	Recursive Least Squares
SoC	System on Chip
SPI	Serial Peripheral Interface
sps	samples per second
TCP	Transmission Control Protocol
THD	Total Harmonic Distortion
TI	Texas Instruments
UART	Universal asynchronous receiver-transmitter

Contents

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Chapter 1

Introduction

The vertiginous advances, registered in the past years in: a) the miniaturization of recording devices; b) the increase of the processing capabilities that have smaller and smaller devices; c) the advances in signal processing (pattern recognition, etc.); and, d) the knowledge of the brain's organization of cognitive functions; have revived interest in developing neural recording systems since the beginning of the last decade [2, 3].

The real time acquisition and analysis of brain signals, either through wearable electroencephalography (EEG) or invasive or implantable acquisition, in order to perform actions or to understand aspects of brain operation, has become scientifically and technologically feasible. The possibility of controlling machines using signals derived from real-time EEG analysis (Brain-Machine Interface, BMI) was conceived by Vidal about 40 years ago [4, 5]. Nowadays, there are multiple initiatives tending to use information of brain activity in products, working stand-alone or in network with other sensors (BSN, Body Sensor Networks) in a wide range of applications, from basic neuroscience research [6–9] to medical clinic [10–14], or from the entertainment industry [15–18] to transport services [19]. There are many opportunities opening up in this field, especially if it is addressed in a multidisciplinary way, including disciplines like neuroscience, computer science, signal processing, information theory and microelectronics, among others.

These applications involve challenges at various levels: 1) in the signal transduction, where electrodes have to "translate" biopotentials generated at cells' membranes into electrical signals suitable to be recorded with an electronic circuit; 2) in the acquisition of the signal, where electronic circuits have to amplify, filter and, eventually, digitize this signal; and 3) in the processing and/or wireless transmission of the signal. An overview of these challenges, from a general-context point of view, starting from the biological basis, will be presented in Chapter 2. In the context of these challenges, the next Section will present the motivation and goals of this thesis.

1.1 Motivation and Goals

As Chapter 2 will show, ultra-low-power consumption, low noise and high common-mode rejection ratio (CMRR) are very desirable features of any biopotential recording system. In some applications, these features are critical. One emblematic example of these applications in the neuroscience domain, is the weakly electric fish neural activity recording, where the interference produced by the discharge of the electric organ of the fish (called electric organ discharge, EOD) is a key factor [20, 21]. Another example, from the implantable devices domain is the nerve activity recorded with cuff electrodes,

where the desired signal is interfered by electromyographic (EMG) potentials generated by muscles near the cuff [22–25]. In these cases, the amplitude of the interfering signals, which mainly appear in common mode, is several orders of magnitude higher than the amplitude of the signals of interest.

Studies of electroreception have provided extensive knowledge about the complete sensory system. Particularly, electrophysiological recordings in weakly electric fish have contributed to the understanding of the system at different levels of organization [6]. This research has provided insights for the understanding of basic questions on brain function in humans and other animals [7, 8, 26], and has bio-inspired man-built autonomous systems (underwater navigation, object classification, communication, etc.) [9]. In these animals, bioelectric potentials can be recorded at: a) single cell level either intra or extracellularly, informing about cell and neural circuit signal integration; b) tissue level (local field potentials, LFP) informing about the average activity of a cell population; and, c) individual level since electrosensory signals, used by the fish for object imaging and communication, are carried by a self generated electric field. For these purposes these animals evolved an electric organ as well as receptors in the skin that are capable of sensing this field.

Weakly electric fish neural recordings are a very challenging task, whether the fish is still in acute experiments or freely-moving. Firstly, the single cell signals (unitary activity) have a spike shape of very low voltage which fire simultaneously with other cells. Thus in order to separate the activity of more than one cell recorded from the same electrode, amplifiers require a resolution in the order of microvolts and very low noise. Secondly, high CMRR is important because the electric field generated by the EOD can also be recorded in the brain. Its amplitude can be more than 1000 times larger than other extracellular signals of interest, so most of the time the EOD behaves as an extra artifact besides the classical ones observed in electrophysiological recordings (powerline and fluorescent lamps ac fields, electrode polarization, etc). Thirdly, to separate different types of LFPs containing slow and fast components from the unitary extracellular activity originated in a single cell, it is necessary to use precise and tuneable bandpass filtering. Finally, freely-moving fish recordings require a small size and weight acquisition system as well as ultra-low-power operation to further reduce size and weight, so that smaller batteries can be used and a reasonable autonomy can be achieved.

The general domain of work of this thesis is the development of techniques for analog integrated circuits targeting applications that require high CMRR and an excellent performance in terms of current-efficiency. We refer to *current-efficiency* to simultaneously achieve low-noise and ultra-low-power over a high bandwidth. Current-efficiency is characterized by the noise efficiency factor (NEF), which will be introduced in Chapter 2. As general guideline, when we state high CMRR, we are thinking of values greater than 80 dB and an excellent performance in terms of current-efficiency implies an input-referred noise level below 2 μVrms and power consumption around 10 μA or less (per channel), operating over a bandwidth greater than 5 kHz, which corresponds to a NEF of 3.4.

The connecting thread of this thesis, will be the design of an integrated neural analog front end (AFE) architecture. Fig. 1.1 shows a block diagram of the circuit. The first stage of the AFE is an amplifier with band-pass characteristic (called *preamplifier*). In Chapter 3 we review the state-of-the-art of preamplifiers and discard the most prevalent architectures. Then, we propose, analyze in depth, implement, characterize in lab, and test in-vivo a novel architecture. The following stages of the addressed circuit include band-pass filters. In Chapter 4 we extend and apply the novel architecture to biquad band-pass filters showing the versatility of the proposed architecture. Next, in Chapter 5 we design an AFE based on the findings of the previous chapters.

Finally, some system-level topics related to signal processing and wireless data transmission will be covered in Chapter 6. In the next section, a detailed thesis outline is presented.

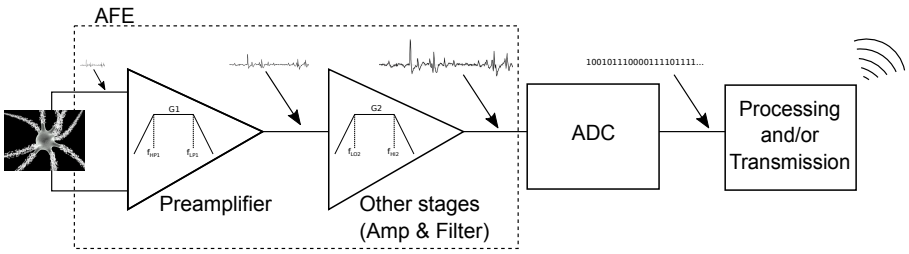

Figure 1.1: A Top-level schematic of a typical neural acquisition system (shown for only one channel and only the acquisition/transmitter side). The neuron depicted in the figure was taken from *Neuron Matrix*. Copyright (c) 2005 Nicolas P. Rougier (released under the GNU General Public License).

1.2 Thesis outline

Chapter 2 provides an overview of biopotential monitoring, from the biological basis to the circuit and system techniques. Signal acquisition, processing and transmission are fundamental capabilities of biomedical research and medical devices development. In these topics, integrated, low power consumption systems for portable, wearable or implantable monitoring of neural signals is taken as study case, presenting both established solutions and research trends. The overview presented in Chapter 2 is an adapted version of [27].

Chapter 3 introduces a novel architecture for neural preamplifiers including silicon implementation, experimental characterization and in-vivo validation. Chapter 3 presents measurement results indicating that our neural preamplifier simultaneously offers low noise (equivalent input-referred noise of 1.88 μVrms), high CMRR (greater than 87 dB) and current-efficiency (NEF = 2.1). Chapter 3 is an extended version of [28]. This chapter also gathers material from [29] as well as unpublished work.

In Chapter 4, we extend and apply the architecture presented in Chapter 3 to band-pass biquad filters. Two filters that meet the same requirements were designed and compared, while the first was based on our novel approach, the second was based on a traditional implementation. Results from Monte Carlo simulations show that the proposed architecture, compared with the traditional one, presents a 30 % reduction in power consumption and more than doubles the dc input that can be blocked. Chapter 4 is an adapted version of [30].

Chapter 5 introduces the design and simulation of an integrated programmable analog front-end architecture formed by the preamplifier presented in Chapter 3 and two additional band-pass amplifying stages based on the filter architecture presented in Chapter 4. Chapter 5 is an extended version of [31]. This chapter also gathers material from [32] as well as unpublished work.

Chapter 6 presents some system-level topics addressed during the thesis, including the design and implementation of three prototypes of end-to-end low-power wireless biopotentials recording systems based on off-the-shelf components. Chapter 6 is based on adapted versions of [33–36].

Chapter 7 summarizes the main findings of this thesis, highlights its main contributions and discusses future works.

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Chapter 2

Biopotential monitoring overview

This Chapter provides a general overview of neural signal monitoring, from the biological basis to the circuit and system techniques. In addition, this Chapter introduces basic definitions that will be used throughout this manuscript and will help to contextualize the main aspects worked on the framework of this thesis. Despite this, a reader who is familiar with the area can skip the reading of this Chapter. This Chapter is an adapted version of [27].

Signal acquisition, processing and transmission are fundamental capabilities of biomedical research and medical devices development. In these topics, integrated, low power consumption systems for portable, wearable or implantable monitoring of neural signals is taken as study case, presenting both established solutions and research trends. Chapter 2 is organized as follows. Firstly, the biopotential sources and the specific requirements for recordings these signals at different levels will be described. Secondly, the design of the front-end circuits, particularly the first amplifying stage, also commonly referred as preamplifier or LNA (low noise amplifier), is considered. This stage must handle the toughest trade-offs in terms of low noise operation and rejection of undesired signals, while keeping consumption at a minimum when battery operated devices are targeted. Thirdly, the problem will be analyzed from the point of view of the biopotential acquisition system as a whole, focusing on wireless systems.

2.1 Biopotential sources

Electrophysiology is one of the most important sources of knowledge on the function of nerve and muscle tissues and the organs that such tissues construct. Some of these organs are involved with transduction of either *in* (sensory organs) or *out* (skeletal, visceral, and heart muscles) signals. Other organs, deal with the transmission (peripheral nerves) and processing of information (the brain and spinal cord) of such signals. Recordings of potential differences generated by excitable cells, provide data on the cell mechanisms of electrogeneration, inform about the localization, timing and waveform generation of biopotential sources and yield insights on the information flow through neural circuits and the activation of different muscle effectors.

The main source of biopotentials is a difference of potential (V) between the inner and outer sides of the cell membrane ranging from 50 to 100 mV. This difference of potential thermodynamically compensates a transmembrane pattern of ion gradients typical for each cell type. Although there are some exceptions, the most used model of cell membrane assumes: the constancy of the electromotive force driving each ion (E) and the relative independence of ion channels conductance though the membrane (g).

As the cell surface is several orders of magnitude larger than its thickness, a constant capacity (C) in parallel is included (Fig. 2.1). Moreover, for the same ion species more than one conductance may be present and show different voltage dependence (i.e. E1=E2 with g1≠g2).

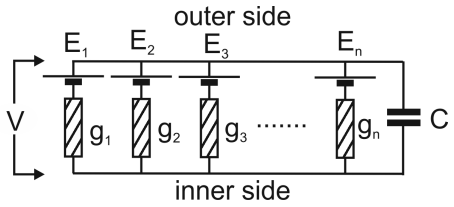


Figure 2.1: Cell membrane electric model.

In addition, ion dependent conductances are a non-linear function of the transmembrane voltage (V), which is in turn, a linear combination of the previous parameters, introducing complex dynamics. Furthermore, biochemical action (and also synthetic drugs) may affect each ion conductance in a different way in different cells.

Biopotentials originated at cells' membranes can be observed at various levels of organization. The basic and most detailed level would be the ionic channels. A key question for researchers interested in pinpointing the mechanisms of cell electrogenesis is to investigate the parameters of each elemental source driving each ionic current. This can be done either by indirectly measuring the contribution of one or several of these sources to the whole membrane voltage [37] or by directly measuring the conductance through isolated ion channels [38]. In both types of experiments a crucial aspect is the capability of recording devices to inject current into the cell and to control such amount of current in order to clamp the voltage either in a constant [37, 38] or dynamic way [39].

As most excitable cells are able to fire fast, all-or-none, events referred to as spikes, the second level of analysis consists in determining the firing time of single cells and their relationships with the firing time of other cells or behavioral events. Each cell is a closed surface (in most but not all cases geometrically spherical). Although the net current through the membrane is zero (Gauss' divergence theorem) any local difference in the transmembrane voltage (due to changes in some ion conductance) causes a localized current between membrane patches of opposite voltage polarity. As the electric field decays with the cube of distance from the emitting source, spikes are recorded only very close to the emitting cell and require electrode recording spots of tenths to hundreds of square micrometers.

The synchronic activity of groups of cells generates larger biopotentials that can be conceived as generated by distributed sources. Depending on the extension of the source and recording distance, two other forms of field potentials can be distinguished: local field potentials arising from the electrical activity of a group of closely located cells and global field potentials arising from the overall electrical activity of a whole structure. These last may be deeply buried in the background activity of other structures and may require to be evidenced by the cross correlation between the raw recorded signals and repetitive events (event related potentials).

Summarizing, different forms of electrophysiological research are focused at different levels of organization: a) to investigate the parameters of each elemental source driving each ionic current to pinpoint the mechanisms of cell electrogenesis; b) to evaluate the timing of activation of single cells by measuring the local currents generated by multiple single cells at the same time; c) to evaluate regional activities of a cell population by recordings of local differences of potential originated in the sum

of currents arising from all neighbor cells; and, d) to record the "noise of the engine" of a whole structure (i.e. the brain, EEG; the heart, electrocardiogram ECG; a group of muscles, surface-EMG) by measuring far field potential differences between points localized out of the structure. Although these approaches mostly rely on measuring the potential difference using electronic amplifiers (which is the focus of this thesis) other signal carriers should be mentioned: i) the magnetic field generated by biogenerated currents (a method used mainly at the organ level) and ii) the luminescence emitted by some substance in the presence of an electric field (a method used mainly at cellular level).

2.2 Specific requirements for recordings at different organization levels

Firstly, different number of channels is required when dealing with different organization levels. In the case of intracellular recordings only a few channels are required but when dealing with the extracellular activities (mentioned above in b, c, and d), it is often necessary to record simultaneously several signals to either assess information transmission between cells, or to compare generators occurring at different positions or orientations. In addition, it is also useful, in many cases, to correlate these signals with behavioral events external to the explored electric sources, imposing a need of additional acquisition channels for synchronism purposes.

Secondly, recording differences of potentials at different organization levels share commonalities, but there are also differences depending on the level and the purpose of the study (Table 2.1). These differences arise from the amplitude and bandwidth of the signals of interest and the electrode characteristics.

Table 2.1: Main electrical characteristic of biopotentials (typical values).

	Bandwidth (Hz)	Amplitude (μV_{pp})	Number of signals
ECG	0.1 - 150	100 - 15000	1-12
EEG	0.03 – 70	20 - 200	4 – 256
EEG (brain stem auditory evoked potential)	30 - 3000	0.05 - 4	2-4 (standard clinical use)
EEG (visual evoked potentials)	0.2- 200	0.5 - 20	2-4 (standard clinical use)
Intracellular recordings	dc - 3000	10 - 250000	1-4
Local field potentials	1 – 500	10 - 5000	1-256
Spikes	0.3 - 5000	50 - 1000	1-256
Surface-EMG	25 - 3000	100 - 1000	1-10

Though a complete treatment of the topic of electrodes is out of the scope of this thesis, the following key considerations are presented. For instance: intracellular electrodes, multiple electrodes (from tetrode to Utah arrays), cuff electrodes and skin electrodes (Ag/AgCl or dry, capacitive, etc.) may behave as additional electric sources in series with the recording system. Usually a linear model of the electrode is sufficient to account their influence on the potential difference recorded by the amplifier, but in the general case, a non-linear model is required. This modeling of the electrode, among other effects, has sometimes to account for up to 100 mV dc signals that can be generated at the skin- tissue- or cell- electrode interface. In the case of intracellular and deep placed extracellular, electrodes glass micropipettes, filled with appropriate

solutions and having a tapered tip adapted to the purpose, have been the standard in the last 60 years [40]. For extracellular recordings of spikes and field potentials, multitrodes have recently improved the ability for recording multiple channels and also to separate several spikes recorded by the same electrode [41].

A particular challenge is posed in order to build small, easy-to-place electrodes and preferably embedded in wearable clothing, when small potentials have to be measured with electrodes in contact to the skin (EEG, EMG, etc.). Standard wet electrodes (Ag/AgCl) are attached to the skin by a conductive gel that improves the interface conditions. This placement process is slow, cumbersome and the result is uncomfortable for the user. On the other hand, dry electrodes have long been known, but their development remains limited to certain niches (fitness, games, etc.). While the main advantages of dry electrodes are their easier placement and use, the quality of the signals acquired with dry electrodes and traditional electronics has significant deficiencies in terms of noise and sensitivity to the electrode movements [42]. Despite this, the use of dry electrodes is clearly growing opening a wide field of research, including optimization methods for electrodes and signal acquisition circuits to alleviate the mentioned disadvantages of dry electrodes.

Third, in the case of freely behaving subjects, unobtrusive biopotential monitoring systems are required. Thus, a target system would be a wearable device (wireless, small and comfortable) with a reasonable autonomy (low-power consumption), capable of acquiring, processing and transmitting biopotential signals. The use of wireless systems grants: a) more freedom to the user or subject under study, since wired systems restrict its movements; b) a simpler setup to the researcher; c) the correlation of the recorded potentials with behavior; and also helps to avoid the interference picked up by long cables between the electrode and the amplifier. There are commercial systems that are approaching to have wireless systems with the characteristics described above and much current research in the design of biopotential monitoring pursues that goal, as will be discussed in the rest of this chapter.

2.3 Challenges in the integrated acquisition of biopotentials

In recent years the trend on this area has been the use of solutions where most (or even all) of the circuitry is included in a single complementary metal oxide semiconductor (CMOS) integrated circuit (IC), instead of what we may call *discrete solutions*, where the circuitry is based on several standard off-the-shelf ICs and passive components. The use of ICs allows for very miniaturized devices that can be unobtrusively placed very close to the recording site (including implantable solutions) as well as to optimize the energy consumption. Following this trend, this chapter will focus on IC solutions because they pave the way for developing a broad range of new applications.

The analog front-end (also referred to as AFE or front-end) is the electronic circuit performing the signal conditioning (amplification and filtering) prior to digitize, process and/or transmit the acquired data (Fig. 2.2).

It is usual to tackle the front-end design with a filtering chain involving an amplifier with band-pass characteristic (preamplifier) and a programmable filtering second-stage [12, 31, 43–49]. Depending on the particular biopotential, it can be necessary that the second-stage provides additional amplification (because of the low amplitude of input signals). On the other hand, if the input signal was sufficiently amplified, the filter may need to deal with linearity issues, specially if rail-to-rail operation is desired in order to accommodate low supply voltages, as is the case in current IC technologies. Second-order roll off (40 dB/decade) is usually sufficient to filter biopotentials. As can

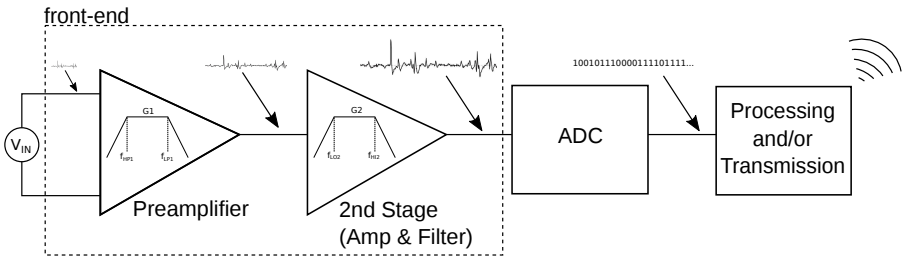


Figure 2.2: Top-level schematic of a typical biopotential acquisition system (shown for only one channel and only the acquisition / transmitter side).

be seen from Table 2.1, cut-off frequencies are usually within the 0.1 Hz to 10 kHz range. Programmability of bandpass filters, which is easily achieved in ICs, is a useful mean for the user to focus the acquisition to the relevant phenomenon. We will turn to the front-end design in Chapter 5.

At the input stage it is advisable to use analog amplification and analog filtering in order to achieve a reasonable signal to noise ratio (S/R) while maintaining energy efficiency [50] as well as providing the needed anti-alias filtering prior to sampling. On the other hand, from the point of view of energy consumption, flexibility and processing performance, it may be convenient to use digital processing in the subsequent stages.

The conditioning circuit is usually followed by a third stage consisting of an Analog-to-Digital Converter (ADC). A typical maximum sample rate is 50 ksps (kilo-samples per second), where samples of 10-bit or 12-bit usually provide an adequate resolution. For instance, a 12-bit ADC with a full scale range VREF = 3 V and a front-end gain $G = 3000$ V/V provides an input resolution of 244 nV with a quantization error of 122 nV. This quantization error is comparable to the equivalent, intrinsic, input noise, which is later presented, therefore higher resolutions would be useless. When several channels are required the ADC may be shared among the channels by multiplexing all or a group of channels at the input.

Some topics related to the final block (processing and transmission) will be discussed in the next section. In the remaining of this section we will focus on the preamplifier, because is the part of the system in closer contact with the biological medium and it has to primary deal with the particular characteristics of the targeted biopotentials.

According to the nature of the biopotentials and the target application, the preamplifier must meet challenging requirements, which usually are contradictory: ultra-low-power consumption, low noise, small size, high input impedance, high CMRR and reject input dc values that are much higher than the input signal amplitude. These challenges are discussed in the next subsections.

2.3.1 Ultra-low-power consumption

Ultra-low-power consumption (up to tens of micro-amps per preamplifier) is a very important requirement in order to operate with small energy sources (in order to reduce size) and to not generate local heating of tissues. Next, it shall be considered how this can be accomplished in integrated implementations. These implementations shall be in CMOS processes, which are at present the prevailing ones and best suited for ultra low power implementations.

The MOS transistor has three regions of operation according to the prevailing mechanism in the current conduction. Firstly, the traditional strong inversion region, where the gate-source voltage is above threshold and the drain current in saturation varies quadratically with the gate-source voltage. Secondly, the weak inversion or sub-threshold region [51], where the gate-source voltage is below threshold and the drain current in saturation varies exponentially with the gate-source voltage. Finally, the moderate inversion, where the gate-source voltage is near or around the threshold region and the drain current in saturation has a mixed behavior. In order to optimize power consumption, the best IC design approach is to exploit all the possibilities that the MOS transistor give us by using indistinctly all its regions of inversion, particularly weak and moderate inversion, because in several cases these provide the best compromise between transconductance generation and parasitic capacitance, leading to an optimum in power consumption [29, 52].

2.3.2 Low noise

The MOS transistors, which are the basic component of these circuits are sources of intrinsic electronic noise, mainly thermal noise and flicker noise. Thermal noise is produced by the random thermal motion of charge carriers, resulting in a power spectral density $S_{TN} \propto 1/g_m$ (independent of frequency), where g_m is the transistor transconductance. Flicker noise is a low-frequency noise related to the charge trapping in the silicon-oxide interface, thus it depends on how the transistor is manufactured, its power spectral density is $S_{FN} \propto 1/f$. The flicker noise can be made negligible in the frequency band of interest through adequate sizing of the transistors or special amplifier design techniques.

The noise added by the preamplifier is modeled as a voltage source $v_{in,rms}$, which is usually referred to the input (equivalent input noise):

$$v_{in,rms} = \sqrt{\int_{BW} S_{in}(f).df} \tag{2.1}$$

where S_{in} is the power spectral density and BW is the bandwidth. $v_{in,rms}$ gathers all the contributions of the preamplifier noisy components.

The noise amplitude added by the preamplifier has to be lower than the biopotentials amplitude in a ratio related to the desired signal to noise ratio. In extracellular recordings this requirement often implies that $v_{in,rms}$ has to be lower than a few micro V_{rms}. As we discuss next, low noise preamplifiers design is ruled by two main trade-offs: noise increases as, on one hand, bandwidth increases and as, on the other hand, power consumption decreases. These dependencies are discussed next.

By definition, the noise is related to bandwidth. When thermal noise is dominant, we have:

$$v_{in,rms} = \sqrt{\int_{BW} S_{in}(f).df} = \sqrt{S_{TN}.BW} \tag{2.2}$$

If the preamplifier input-stage is implemented with a differential pair operating in weak inversion and these transistors are the only source of noise (noise contributions of other transistors are made negligible):

$$v_{in,rms} = \sqrt{S_{TN}.BW} \propto \sqrt{\frac{BW}{g_m}} \Rightarrow v_{in,rms} \propto \sqrt{\frac{BW}{I_{DD}}} \tag{2.3}$$

where $v_{in,rms}$ is the preamplifier input-referred noise, BW is the bandwidth and I_{DD} is the total supply current. Eq. 2.3 highlights the noise-consumption trade-off

and the noise-bandwidth trade-off. For instance, in order to decrease 10 times the noise level, it will be necessary to increase 100 times the current consumption.

In order to quantify the current consumption efficiency in achieving low noise at a given bandwidth, as well as guide design decisions, the following NEF (noise efficiency factor) is a figure of merit that is widely used in integrated biopotential amplifiers (the lower it is the better) [53]:

$$NEF = v_{ni}\sqrt{\frac{I_{DD}}{2k\pi TU_T BW}} \tag{2.4}$$

where v_{ni} is the input-referred noise voltage, I_{DD} is the total supply current, BW is the bandwidth, $U_T = kT/q$ is the thermal voltage, k is the Boltzmann constant, T is the absolute temperature and q is the electron charge.

Another figure of merit, the PEF (power efficiency factor), is usually used [54]:

$$PEF = NEF^2 \times V_{DD} \tag{2.5}$$

In battery powered systems (or powered through a linear regulator) the most relevant metric of consumption is the charge (or equivalently the current) drained from the battery. In these cases, the current-efficiency characterized by the NEF is the most appropriate figure of merit. When the amplifier is powered through a switched dc/dc converter, the power is the most relevant metric to assess consumption, since once we assume a given efficiency of the converter and battery voltage, the current consumed from the battery will be mainly determined by the power consumed by the amplifier. In this case, the power-efficiency, which can be assessed through the PEF, is the most appropriate figure of merit. Nevertheless, it must be noted that the PEF is strongly dependent on the supply voltage of the circuit, which in turn is dependent on the manufacturing process and its threshold voltages. Finally, It must be noted that PEF is heavily dependent on the circuit topology because not all topologies can be scaled due to headroom limitations.

2.3.3 Small size

Size is largely reduced by resorting to integrated implementations. Nevertheless, size reduction in integrated form is mainly limited by two factors. On the one hand, the integration of large time constants (associated with the low frequency of biopotentials) tend to require large capacitors, which occupy large silicon area. On the other hand, the increasingly need to record more and more channels. This requirement would not be an issue regarding the silicon area if the preamplifier could be shared with multiple electrodes through an analog multiplexer. However, the large time constants involved in the preamplifier prevent a fast enough changeover of the preamplifier among channels, leading to the need of one preamplifier per channel [55].

2.3.4 High input impedance

High input impedance is necessary in order to guarantee that the output impedance of the electrode and/or the electrode-tissue impedance do not significantly affect the signal conditioning. This requirement is critical when one electrode is connected to several amplifiers, for example the reference in a multichannel recording. Depending on the application, the output impedance of electrodes, in the frequencies of interest, ranges from a few kilo-ohms (i.e. wet EEG electrodes) to several mega-ohms (i.e. dry EEG electrodes). In the case of dry electrodes, is very challenging that the front-end input impedance (including connections and packages) be actually much higher than the electrode output impedance, thus some small signal degradation might occur.

2.3.5 High CMRR

Biopotential monitoring require to separate the low-amplitude signals of interest from other biological or external interfering signals appearing in common mode. A CMRR greater than 80 dB [20–25] is required because these common mode interfering signals can have amplitudes much more larger than the monitored biopotential. The high CMRR requirement becomes critical in the acquisition of low amplitude extracellular biopotential in which the signal waveform carries significant information.

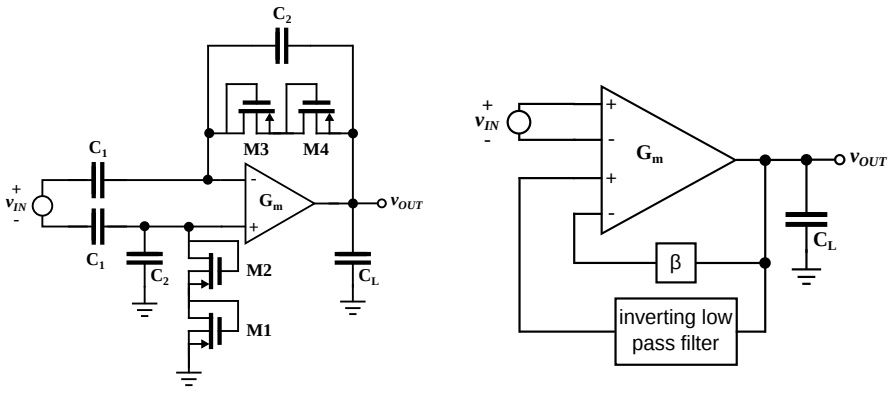
2.3.6 Reject dc input signals

The tissue-electrode interface develops undesired dc voltages which are superposed to the low-amplitude biopotential of interest. In neural recordings these dc signals are typically in the range of 1 mV - 10 mV, and can be up to a maximum of 50 mV [56]. In other recordings, 100 mV o even higher input dc voltages values can be found. To avoid such artifact, it is possible to use capacitors between the electrode and the preamplifier to eliminate the dc voltage, leading to an *ac-coupled circuit*. Due to the slow-nature of biopotentials, this option requires large capacitors or large resistors, which can't be integrated because occupy a large silicon area. One way to overcome this problem is to use MOS-bipolar pseudo-resistors [57]. The pseudo-resistor can be thought as a transistor "almost off", that presents a very high resistance. In contrast, the resistance of this nonlinear element is difficult to model and control, and can also suffer from drift [49, 58, 59]. Alternatively, there are *dc-coupled circuits* that rely on feedback instead on capacitors for eliminating the undesired dc voltage.

2.4 Main biopotential integrated preamplifier architectures

Harrison et al. in [57] present a bandpass preamplifier architecture that in the last decade has become a very important reference, widely applied [43–49, 60–70]. At that time, [57] reported the best noise-consumption compromise, and in some aspects the circuit is still in the state-of-the-art of biopotentials amplifiers. The core of Harrison's circuit (see Fig. 2.3a) is a resistor-less differential amplifier based on a symmetrical operational transconductance amplifier (OTA). To minimize noise, this architecture relays in a careful design of all the OTAs transistors, particularly those of the input differential pair (using wide transistors, working in weak inversion). The circuit has several interesting aspects: the gain is set by a ratio of capacitors, avoiding the use of resistors which are a source of noise and consumption; has differential input, and the high-pass characteristic, which requires high valued resistors, is defined by MOS-bipolar pseudo-resistors (M1, M2, M3 and M4 in Fig. 2.3a). Therefore, although high-pass frequencies less than 0.1 Hz can be reached, this can only be done with low accuracy. Two workarounds on this problem have been proposed. In the first place, to set the high-pass frequency by the next stages [66], which jeopardize power consumption and area, among other important features. In the second place, to modify the pseudo-resistor arrangement so that the equivalent resistance can be controlled through the gate voltage of the MOS transistors that operate in weak inversion [71]. This allows for an off- or on-chip tuning of the high-pass frequency. However, even if the accuracy issue is solved, a second drawback remains. This drawback is the intrinsically low CMRR, which is limited by the capacitor matching (we elaborate on this in Section 3.2.3). Then, while acceptable values of CMRR (60 dB) are obtained, it is not possible to guarantee very high values (greater than 80 dB).

Other biopotential amplifier architectures, which have not had as much impact as Harrison's, have been proposed over the years. An important subset of these, uses a



(a) Harrison et al. [57] (b) Based on a DDA [72, 73].

Figure 2.3: Main biopotential integrated preamplifier architectures.

differential difference amplifier (DDA) [72] as input stage [58, 73–79], while others are based on different approaches [53, 80–84]. A DDA is composed of an OTA with two added differential inputs. One architecture [73] for implementing an instrumentation amplifier by means of a DDA is shown in Fig. 2.3b. It uses one differential input for the signal to be amplified, and the other differential input for the feedback that sets the gain (feedback factor β) and high-pass characteristic (inverting low-pass filter). This architecture, as discussed in Section 3.2.3, is intrinsically suitable for high CMRR, and the gain and bandpass cut-off frequencies are set by means of parameters that are, respectively, very accurate (i.e. ratios of transconductances) or can be easily and automatically tuned (i.e. ratios of transconductance over capacitances) [85], achieving high accuracy without jeopardizing power consumption [86]. However, a straightforward implementation of a DDA adds an important amount of noise and consumption (because of the two OTAs at the input).

This topic, including an in-depth study of the state-of-the-art of preamplifiers, will be taken up in Chapter 3.

2.5 Challenges for wireless multichannel biopotential recording systems

The most important challenge that faces the design of wireless biopotential recording systems is handling an enormous amount of information that is generated in a small device, with severe power and processing constraints. To acquire signals of 10 kHz bandwidth, a minimum sampling frequency of 20 ksps/ch is required. Then, 8 channels and 12-bit samples imply an effective data throughput of 1.92 Mbps (Mega-bit per second). If it were 100 channels, the effective data rate should be greater than 24 Mbps. No low-power wireless standard communication protocol reaches these transmission rates nowadays.

In the last 20 years, there have been several proposals for providing a solution for solving this problem [87, 88]. [87] present a discrete two channel system for acquiring flying locusts EMG signals. The acquired analog signal is directly transmitted in the 145 MHz band within a range of 20 meters. The system weighs 0.55 grams and has 7.3 hours autonomy powered from a 1.5 V battery, which is overall an impressive

performance for the date it was designed and not using custom integrated circuits. [88] present an integrated four channel telemetry system, which acquires neural signals and EMGs in flying locusts and weakly swimming electric fish, and transmits them wirelessly in the 900 MHz band within a range of 2 meters. The samples are digitized with 9 bits and the useful date rate is 104 kbps (kilo-bit per second). The system weighs 0.17 grams and has 5 hours autonomy powered from a 1.5 V battery. Table 2.2 presents some selected examples of commercially-available wireless biopotential recording systems.

Table 2.2: Commercial wireless biopotential recording systems.

Application	Neural Recording	EEG	EEG	EEG/EMG
Number of channels	128	64	8	64
Weight (grams)	12	800	360	500
Autonomy (hours)	1-3	12-24	25-100	5
Effective data rate	25 ksps/ch	4 ksps/ch	0.3 ksps/ch	2 ksps/ch
Input-referred noise	8.5 μV_{rms}	2 μV_{pp}	N/A	1 μV_{rms}
Communication protocol	Proprietary, analog 4-meters range	WiFi	Bluetooth 2.0	WiFi
Manufacturer	Triangle	Natus	g.tec	ANT Neuro
Model/Series	W-series [89]	Nicolet [90]	g.Mobilab+ [91]	eego rt [92]

N/A=Not available

Regarding digital communication, it is important to distinguish between effective data "rate" and "raw data rate". The effective data rate (also named useful data rate) refers to the information that the user or the application need to receive or transmit. The raw data-rate (also referred as the over-the-air data rate) is the total number of transferred bits per second over the communication link, this data-rate takes into account not only the useful data, but also any other transmitted data (i.e. protocol overhead). Some digital wireless communication standards are discussed next.

Typical implementations of Bluetooth (BT) and its low-power version "Bluetooth low energy" (BLE), are designed to operate in short distances (from a few meters to several tens of meters). BT can achieve an effective data rate of up to 800 kbps while consuming an average current in the order of 20 mA. BLE typically achieves a maximum effective data rate of 200 kbps while consuming an average current less than 10 mA. These protocols typically communicate two devices (host and client), don't require infrastructure and are easy to install and configure.

The IEEE 802.15.4 standard specifies the low level layers of a low power (less than 10 mA), low effective data rate (up to 50 kbps), and short distance (from a few meters to several tens of meters) wireless communication protocol. Zigbee is a protocol based on this standard. These protocols typically communicate several devices (sensor nodes) and don't require infrastructure since they organize "ad hoc" networks.

In the same range of distances, options like WiFi, can be used to monitor biopotentials. In this case, an effective data rate of 5 Mbps is easily achieved, but current consumption of hundreds of milliamperes has to be tolerated. WiFi typically communicates several devices by means of additional infrastructure (i.e. router).

A promising way to solve the problem of having to transmit such a high volume of data is to incorporate data processing to reduce the amount of transmitted data [93]. In some applications, the data processing consists of methods for detecting the relevant information contained in the biopotential signal. To illustrate this, let us consider the particular example of the detection of the spikes that indicate neurons activation, where several methods for reducing the amount of information to be transmitted have

been proposed. Some of them, compare the acquired signal against a template (called "template matching"). These methods are particularly effective when the waveform of the target spike is known or can be estimated. There are also methods which measure (and transmit) the energy of the signal [94]. Although in many cases it is sufficient to send the inter spike interval, there are works that have proposed to send more data (without sending the complete stream). For example, in a "feature extraction" data compression scheme, where the spike is detected by two thresholds (one negative and one positive), and instead of sending the complete signal, either a short epoch of about 2 ms long including the spike waveform or a few points can be transmitted [47].

An alternative approach is to apply general data compression techniques, which have been proposed in the past 20 years. Methods ranging from simple dictionary-based approaches to more sophisticated context modeling techniques, methods that exploit the biopotential particularities (i.e. temporal and/or spatial correlation) or methods that don't [95–97]. In Chapter 6 will be presented the implementation of a compression algorithm in a microcontroller-based low-power platform.

Another way to deal with a high volume of data, is to perform some data processing in order to take decisions "in situ" (for example to give an alarm or to stimulate), thus completely avoiding the need to transmit data [49, 98].

The acquisition of biopotentials in synchrony with a stimulus signal is a challenge that is not fully solved. In several research areas related to neurosciences, medicine or psychology, among others, it is important to record biopotentials after performing a certain stimulus (visual, auditory, etc.) in order to search for correlations. To have a system that offers to the user, a stimulus signal perfectly synchronized with the signal under observation, is a problem not completely solved today.

We will taken up with practical aspect of this topic in Chapter 6, when presenting the implementation of three wireless biopotential recording systems based on off-the-shelf components developed in the framework of this thesis.

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Chapter 3

Design and implementation of a neural preamplifier

As discussed in Chapter 2, the preamplifier is probably the most important part of the recording system, because it is the part of the system in closer contact with the biological medium and it has to deal with the particular characteristics of the targeted signals. In this chapter we review the state-of-the-art of preamplifiers and discard the most prevalent architecture. Then, we propose, analyze in depth, implement, characterize in lab, and test in-vivo a novel architecture. This chapter is an extended version of [28], and also gathers material from [29] as well as unpublished work.

3.1 State-of-the-art of neural preamplifiers

This review will focus on noise performance, current-efficiency, and CMRR, which are the main features of our recording system. As will be discussed in Section 3.2.3, in order to correctly compare CMRR performance, it is important to consider the effects of matching. For this reason, it is incorrect to report the typical value of a simulation. In our opinion, experimental measurements jointly with the worst-case value in a Monte Carlo (MC) simulation is a correct manner to characterize CMRR. Next, when we state a CMRR performance it will correspond to a measured value (or the worst-case if more than one chip was measured), in those works where the CMRR worst-case simulation is reported it will be explicitly indicated.

As presented in Section 2.4, Harrison et al. proposed in [57] a neural preamplifier architecture featuring an input-referred noise $v_{ni} = 2.2\ \mu\mathrm{V}_{rms}$, NEF = 4.0, CMRR = 83 dB, and a CMRR worst-case simulation of 42 dB. This architecture has been widely applied to the design of preamplifiers [43, 49, 61, 62, 64–70, 81], front-ends or complete recording systems [44–47, 62, 65, 66], as well as to more complex recording system with integrated signal processing, like spike detection or data compression [47, 49, 60, 63, 67]. Some of these works will be briefly reviewed next.

Horiuchi et al. [60] present a circuit featuring a spike detection scheme based on thresholds including a preamplifier with a remarkable low-power consumption ($I_{DD} = 530$ nA), but not good enough in terms of the parameters we are analyzing ($v_{ni} = 20.6\ \mu\mathrm{V}_{rms}$, NEF = 7.1 and CMRR is not reported).

Wattanapanitch et al. [61] present a modification to the architecture proposed by Harrison et al. that consists in a folded-cascode structure in the transistors of the input differential pair, this allows to reduce the power consumption. This circuit has

a very good performance (v_{ni} = 3.06 μV_{rms}, NEF = 2.67 and CMRR = 66 dB) but presents a narrow bandwidth (45 Hz - 5.32 kHz).

Zou et al. [43] propose improvements to the Harrison et al. architecture, in particular, a technique to improve the linearity of the pseudo-resistors. This work achieves a good performance (v_{ni} = 2.5 μV_{rms}, NEF = 3.26 and CMRR = 71.2 dB), but working on a much more limited bandwidth (4.5 mHz - 292 Hz).

Bonfanti et al. [63] present a 16-channel neural recording system featuring data compression (implemented by detecting the spikes and storing up to 20 points for each waveform) and wireless transmission. The preamplifier is a straightforward implementation of [57] where the main OTA was implemented as a single-stage telescopic cascode amplifier and a second-stage Gm-C filter set the high-pass frequency. This work achieves a very good performance (input noise v_{ni} = 3.05 μV_{rms}, NEF = 2.5 and CMRR = 65 dB)

Wattanapanitch et al. [45] present a 32 channels front-end, where the first stage is based on [61]. The preamplifier of this new version is not as good in terms of the parameters we are analyzing (input noise v_{ni} = 5.4 μV_{rms}, NEF = 4.4 and CMRR = 62 dB) but is much better in terms of area (0.03 mm^2 per amplifier).

Al-Ashmouny et al. [46] present a 128 channels neural recording system, where the design of the OTA preamplifier explores the moderate inversion region for some transistors (the current mirror of the first stage and other transistors of the second stage). The overall system presents a good performance (v_{ni} = 4.8 μV_{rms}, NEF = 2.9 and CMRR = 62 dB).

Abdelhalim et al. [49] present a 64-channel wireless recording system including a neurostimulator. The front-end is implemented in two stages. The preamplifier presents a good performance (v_{ni} = 5.1 μV_{rms}, NEF = 4.4 and CMRR = 71.5 dB). The second stage, based also on the Harrison et al. architecture, set the high-pass frequency by tuning the MOS pseudo-resistors.

Liu et al. [69] present a 64-channel neural recording system. The preamplifier uses a folded-cascode topology featuring an overall very good performance (v_{ni} = 3.86 μV_{rms}, NEF = 2.8 and CMRR = 69 dB).

Several works [47, 64–66, 68] have implemented the Harrison et al. architecture jointly with a "current reuse" technique [62], which consist in a complementary input differential pair to reuse the tail current and nearly double the achieved transconductance (both input NMOS and input PMOS transistors are stacked in the same current branch). Next we review some of them.

Rodríguez-Pérez et al. in [47] present a neural recording channel with spike detection and a data compression scheme based on feature extraction. The preamplifier introduces two additional interesting modifications to the original architecture. Firstly, it uses a fully-differential architecture to increase the dynamic range of the preamplifier and improve the PSRR (Power Supply Rejection Radio) and CMRR performance. Secondly, it implements a low-pass filter of 40 dB/dec in the input stage, enabling a reduction of the input noise. This preamplifier achieves a very good performance (v_{ni} = 3.8 μV_{rms}, NEF = 2.26 and CMRR = 83 dB). In [70] additional data of this preamplifier is reported.

Wang et al. [68] present a preamplifier where floating-gate transistors are employed for tuning the high-pass frequency and to implement the common-mode feedback block. The circuit has a very good performance (v_{ni} = 2.8 μV_{rms} NEF = 2.25 and CMRR = 70 dB).

Chae et al. [64] present a wireless neural recording system with on-chip processing and in-vivo measurements (v_{ni} = 4.9μV_{rms}, NEF=1.92 and CMRR=90dB). However, since the work is presented from a system-level point of view, key results of the pream-

plifier are missing[1]. Firstly, simulations or measurements of the preamplifier frequency response are not reported. Secondly, it is not mentioned how a 90 dB of CMRR is achieved (and as it will be discussed in Section 3.2.3, this value of CMRR requires -at least- very high levels of matching between the capacitors that set the gain). Finally, there is no measurements nor MC simulations of the CMRR spread with frequency.

Han et al. [65] introduce a 100 channels neural recording system where the fully-differential preamplifier achieves a very good overall performance (v_{ni} = 3.2 μV_{rms}, NEF = 1.57 and CMRR = 73dB), in this case with a remarkable 0.45 V power supply.

Zou et al. [66] present a 100 channels neural recording system. The high-pass frequency of the system is determined by a second-stage band-pass filter. Despite the poor CMRR value, this preamplifier achieves a very good performance (v_{ni} = 4.0 μV_{rms}, NEF = 1.9 and CMRR = 60 dB).

In order to correctly compare input noise, NEF and PEF performance, it is important to consider the adequate noise integration bandwidth. For instance, the noise integration bandwidth of Chae et al [64], Han et al. [65] and Zou et al. [66] only covers the amplifier bandwidth. If the low-pass filter were ideal, it would be correct, but the roll-off of these works is -20 dB/dec. This led us to the conclusion that the actual input noise of these works is, at least, $\sqrt{\pi/2} = 1.25$ times higher, which implies an actual NEF $\geq$ 2.0 in all cases.

As mentioned in Chapter 2, and confirmed by the previous review, an important drawback of the Harrison et al. architecture is the intrinsically low CMRR. A few works achieve a CMRR value higher than 80 dB, and the CMRR worst-case value is rarely reported (and when it is, the reported value is much smaller than the measured one). For this reason, the Harrison et al. architecture is not suitable in our applications.

Other architectures have been proposed over the years. An important subset of these uses a DDA [72] as input stage [58, 73–77], while others are based on different approaches [53, 80–84]. Some of them will be reviewed next.

Ng et al. [81] present a 16 channel analog front-end. The input impedance mismatch problem (which arises when several inputs are acquired with the same reference) is addressed by using single-ended CMOS-inverter-based preamplifiers for both the reference and signal inputs. The CMOS-inverter inherently incorporates the previously mentioned "current reuse" technique. The second stage, which is a straightforward implementation of the Harrison et al. architecture, provides additional amplification. A third stage set the high-pass frequency through an externally applied dc voltage. The CMRR is measured under different conditions, the worst case value reported is 46.1 dB. The noise integration bandwidth only covers the amplifier bandwidth. The circuit has a good performance (v_{ni} = 4.1 μV_{rms}, NEF = 3.19, CMRR = 80 dB).

Chatuverdi et al. [83] use an open-loop single-stage amplifier instead of a closed-loop configuration. The inherent gain inaccuracy of the open loop architecture is compensated by using a variable gain amplifier in the second stage (which is not implemented). The overall performance is good (v_{ni}=5.5μV_{rms}, NEF = 2.6, CMRR not reported).

Guo et al. [82] presents a fully-differential preamplifier. The input block is a symmetrical OTA with a source degenerated input differential pair. This block is followed by a variable gain stage and a feedback loop (composed by an integrator and an OTA) that determines the low frequency characteristic. Chopping is used to lower the low frequency noise. By tuning a pseudo-resistor in the integrator, the high-pass frequency can be adjusted (as this pseudo-resistor is not in the signal forward path, its non-linearity does not affect the preamplifier linearity). This work exhibits a very good performance in terms of linearity (a total harmonic distortion THD of 0.1% with an

[1]These results are also not reported in other papers of the same authors related to the same preamplifier [99–101].

input of 20 mV_{pp}), CMRR (despite the worst-case value is not reported, a measured one of 110 dB it is) and noise (v_{ni} = 2.9 μV_{rms}). However, its current-efficiency (NEF = 6.6) makes it not appropriate for our applications.

The performance achieved by relevant prior works that present a good performance in terms of CMRR, input noise and NEF are compared with our work in Section 3.4.3.

The solution proposed in this thesis will follow the lead of DDAs. As mentioned in Section 2.4 and further discussed in Section 3.2.3, a DDA is intrinsically suitable for high CMRR, and the gain and band-pass cut-off frequencies are set by means of parameters that are, respectively, very accurate or can be tuned without jeopardizing power consumption. However, a straightforward implementation of a DDA adds an important amount of noise and consumption (because of the two OTAs at the input).

3.2 Proposed solution

Our solution aims to overcome the drawbacks presented by Harrison et al. architecture and standard DDAs in order to obtain a neural amplifier with high CMRR, low input noise and current-efficiency. Our starting point is a variant of the architecture proposed in [58] shown in Fig. 3.1. This architecture proposes a DDA input stage composed of two symmetrical OTAs shown as Gm1[2] and Gm2, and a feedback factor β, where the transconductance of Gm1 (G_{m1}) is higher than the transconductance of Gm2 (G_{m2}). If a standard DDA is used ($G_{m1} = G_{m2}$), the noise of Gm2 contributes to the input as much as the noise of Gm1. By making $G_{m1} > G_{m2}$, the noise contribution of Gm2 can be made negligible. A possible drawback of this architecture arises from the reduction of the current provided by Gm2 to the summing node with respect to the current provided by Gm1. This reduction decreases the range of dc currents at the Gm1 output that the feedback through Gm2 can compensate. When this compensation is not possible the circuit loses its high-pass characteristic. This was solved by setting the high-pass frequency of the preamplifier (and compensating the aforementioned dc component) through a local feedback at the output of Gm1, which is discussed in the next section. The summing block is obtained just connecting the two OTAs outputs and thus adding their output currents, and β is set to 1.

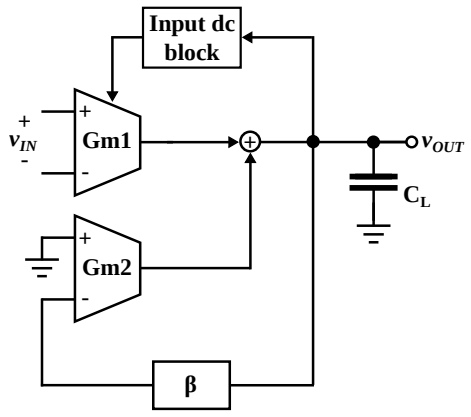


Figure 3.1: Block diagram of the architecture proposed in [58].

Fig. 3.2 shows the novel architecture proposed in this work. An efficient and

[2]OTA notation: Gmi refers to the block, G_{mi} (italic) is the transconductance of the block and g_{mi} (italic lowercase) is the transistor transconductance.

simple single-stage circuit for the preamplifier main transconductor (Gm1) is one of the contributions of this work. Gm1 core is formed by M1, M2, M3 and M4. The M5-M8 block jointly with Gmf and C_F, implement the output feedback loop that establishes the high-pass characteristic and blocks the dc input. Gm2 and Gmf are symmetrical OTAs whose respective transconductances are G_{m2} and G_{mf}. $g_{m2} = K_{G_{m2}} G_{m2}$, where $K_{G_{m2}}$ is the copy factor[3] of the current mirrors of Gm2, as indicated in Fig. 3.2, and g_{m2} is the transconductance of input transistors of Gm2. In the same way we will introduce $K_{G_{mf}}$ such that $g_{mf} = K_{G_{mf}} G_{mf}$ and g_{mf} is the transconductance of the input transistors of Gmf. We use symmetrical OTAs because it is a simple architecture, but other alternatives could be considered. However, a single-stage circuit, like the one used in Gm1, is not suitable to accommodate the required input and output ranges of Gm2 and Gmf. Furthermore, the saving on power consumption due to the use of a single-stage circuit in these blocks has little impact.

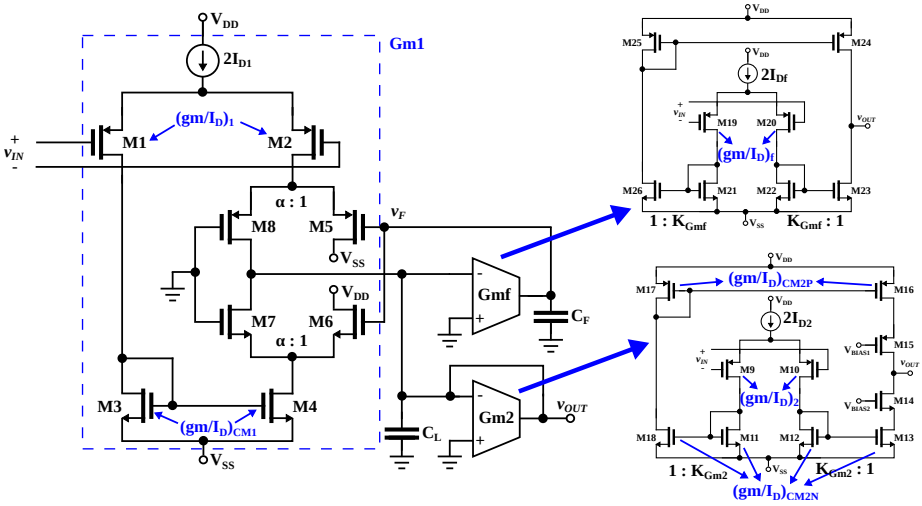


Figure 3.2: Block diagram of the proposed architecture. M1-M4 are the main transconductor (Gm1) core. High-pass characteristic is set through M5-M8, Gmf and C_F. Gm2 and Gmf are implemented with symmetrical OTAs.

3.2.1 Transfer function

Gm1 is an OTA with a differential input (v_{IN}) and a single ended input (v_F). This single ended input is used in the local feedback loop at the output for dc blocking. In small-signal operation it can be useful to interpret M7-M6 and M8-M5 as asymmetrical differential pairs where α defines the degree of asymmetry (see Fig. 3.2): $g_{m7} = \alpha g_{m6}$ and $g_{m8} = \alpha g_{m5}$, where g_{m5}, g_{m6}, g_{m7} and g_{m8} are the transconductance of M5, M6, M7 and M8 respectively. As will become clear in Section 3.2.2, an $\alpha \gg 1$ is adopted, which implies that $g_{m7} \gg g_{m6}$ and $g_{m8} \gg g_{m5}$. Therefore, the transfer function of Gm1 is as follows (see Fig. 3.2):

$$i_{Gm1} \cong G_{m1} v_{IN} + (g_{m5} + g_{m6}) v_F \tag{3.1}$$

[3]To have values of K greater than 1, the copy factor is defined as the inverse of what is the usual way to do it.

where G_{m1} is the Gm1 transconductance ($G_{m1} = g_{m1}$ where g_{m1} is the transconductance of M1 and M2).

The circuit depicted in Fig. 3.2 has the first-order band-pass transfer function presented in Eq. 3.2 (see demonstration in Appendix A),

$$\frac{v_{out}}{v_{in}} = \frac{\frac{G_{m1}}{C_L}s}{s^2 + \frac{G_{m2}}{C_L}s + \frac{(g_{m5}+g_{m6})G_{mf}}{C_L C_F}} \tag{3.2}$$

and the low-pass frequency $f_{low-pass}$ is given by Eq. 3.3, the band-pass gain G by Eq. 3.4 and the high-pass frequency $f_{high-pass}$ by Eq. 3.5,

$$f_{low-pass} = \frac{G_{m2}}{2\pi C_L} \tag{3.3}$$

$$G = \frac{G_{m1}}{G_{m2}} \tag{3.4}$$

$$f_{high-pass} = \frac{(g_{m5} + g_{m6})}{G_{m2}} \frac{G_{mf}}{2\pi C_F} \tag{3.5}$$

3.2.2 High-pass / input dc block circuit

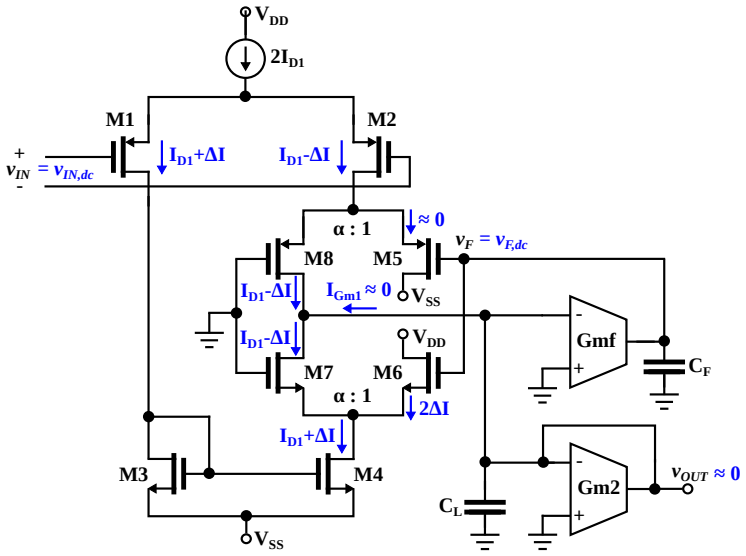


Figure 3.3: Block diagram of the proposed architecture. The steady state condition of the input dc blocking mechanism is highlighted: a dc input signal $V_{IN,dc}$ makes that the current by M8 be equal to $I_{D1} - \Delta I$ and the current by M7 equal to $I_{D1} + \Delta I$, resulting that $I_{Gm1} = -2\Delta I$. Then v_{OUT} falls (Gm2 acts as a resistor to ground), Gmf increases its output current and v_F rises, making M5 to drain less current so that in the steady state condition the current by M5 is approximately 0 and the current by M6 is approximately $2\Delta I$. This equilibrium implies that the current by M8 equals the one by M7 and $I_{Gm1} \approx 0$.

Fig. 3.3 shows the schematic of Gm1. In an OTA standard structure (without M5 and M6) M7 and M8 would be ordinary cascode transistors, but in this circuit they also perform another function. Jointly with M5 and M6, which are in charge of draining the excess current caused by a dc input signal, they are the core of the input dc block or high-pass circuit.

Considering dc operation, the current by M1 and M2 is ID1. Any dc input signal $V_{IN,dc}$ will generate a current ΔI through M1 and M2 (see Fig. 3.3), that will be copied to the output by the current mirror formed by M3 and M4. Then, if M5 and M6 are not present, this current will flow by M7 and M8 and will exit the circuit at the output node.

The M5-M8 block, jointly with Gmf and C_F, are dedicated to establish the high-pass characteristic and to block the dc input. Indeed, the aforementioned ΔI current at the Gm1 output (I_{Gm1}) will be compensated by M5 or M6, in order to keep the output voltage v_{OUT} equal to zero, via the integrator Gmf-C_F.

For instance, when the dc input signal causes the current by M8 ($I_{D,M8} = I_{D1} - \Delta I$) to fall (or equivalently causes $I_{D,M7} = I_{D1} + \Delta I$, the current by M7, to rise), $I_{Gm1} = -2\Delta I$ will fall, then v_{OUT} will fall as well (Gm2 acts as a resistor to ground). Then Gmf will increase its output current and v_F will rise, making M5 to drain less current (or equivalently making M6 to drain more current). The equilibrium will be reached when $I_{D,M7} \approx I_{D,M8}$ or consequently when $I_{Gm1} \approx 0$. This steady state condition (marked in blue in Fig. 3.3) holds in a simplified case where Gmf-C_F provides ideal integration with infinite dc gain. In a practical case the finite dc gain and offset of Gmf will result in a small remaining output dc offset. A similar reasoning can be carried out if $I_{D,M8}$ rises (or equivalently $I_{D,M7}$ falls).

It is interesting to note that any mismatch present in the transistors of Gm1, that can generate a ΔI current, will also be minimized by means of this technique.

One side-effect of this technique is that in ac operation M5 and M6 will drain signal current. Then, if a high level of dc input must be blocked, a loss of gain will be registered. An alternative to overcome this problem is to size M5-M8 in a way that $g_{m7} \gg g_{m6}$ and $g_{m8} \gg g_{m5}$ ($\alpha \gg 1$). For this reason, α is a key parameter in the design process. On the one hand, if $\alpha = 1$, the differential pair will be symmetrical, half of the gain will be lost in M5 and M6, and the circuit will be able to block higher levels of dc input signals. On the other, if $\alpha = 100$ or greater, the loss of gain will be negligible, but the capacity of blocking high levels of dc input signals will be reduced (this is later quantified in Table 3.5).

3.2.3 CMRR

If we consider the architecture proposed by our work, we have:

$$CMRR = CMRR_{OTA} \tag{3.6}$$

where $CMRR_{OTA}$ is the CMRR obtained by the transconductor Gm1 (which can be as high as it can be on any OTA), which can be modeled with the circuit depicted in Fig. 3.4.

In this structure, there are two factors that reduce the common mode gain [102, Section 4.3.5.3]. The first factor is the intrinsic rejection of common mode signals (low common mode gain) of a differential pair structure. The common mode gain of each branch of the OTA input stage is given by $R_L/2.r_{tail}$, where R_L is the load resistance and r_{tail} is the resistance of the "tail" current source of the differential pair. It is worth noting that r_{tail} could be designed to be high by well known techniques, like cascoding it. The second factor is the common mode attenuation due to symmetry. If the structure were perfectly symmetrical (i.e. without systematic or random mismatch), the common mode gain would be zero. When mismatch is considered, the common mode gain is

$$A_{OTA}^{CM} = \frac{R_L}{2.r_{tail}}(\epsilon_d + \epsilon_{cm}) \tag{3.7}$$

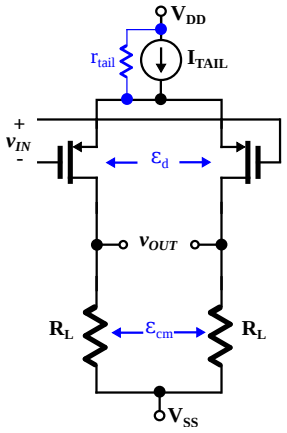


Figure 3.4: Simplified model of the input stage of an OTA.

where ϵ_d and ϵ_{cm} are asymmetry error coefficients due to mismatch of the differential pair and current mirror respectively (in Section 3.2.5, the reason why these coefficients are small in our architecture is discussed).

If we consider the amplifier proposed by Harrison et al. [57, Fig. 1], the CMRR can be expressed as [103]:

$$\frac{1}{CMRR} \cong \frac{1}{CMRR_{OTA}} + \frac{1}{CMRR_{mismatch}} \tag{3.8}$$

where $CMRR_{OTA}$ is the CMRR of the OTA and $CMRR_{mismatch}$ is the resulting CMRR due to the mismatch of passive elements (capacitors C1 and C2, if we consider in-band frequencies) considering the OTA has infinite CMRR ($CMRR_{OTA} \to \infty$).

From Eq. 3.6 and Eq. 3.8 it can be concluded that the CMRR of the architecture of [57] is always worse than the one obtained by our architecture. Additionally, it is usually met that $CMRR_{OTA} > CMRR_{mismatch}$, thus $CMRR_{mismatch}$ dominates Eq. 3.8. The reasons for this are, firstly, the OTA open loop differential gain is much larger than the closed loop one. Secondly, as will be shown next, the OTA common mode gain A^{CM}_{OTA} is lower than $A^{CM}_{mismatch}$.

Following a similar reasoning of [103] it can be seen that the worst-case of $CMRR_{mismatch}$ is:

$$CMRR_{mismatch} \cong \frac{1 + C1/C2}{2(\delta_1 + \delta_2)} \tag{3.9}$$

where δ_1 and δ_2 are the tolerance of C1 and C2 respectively[4], and the worst-case of the common mode gain is:

$$A^{CM}_{mismatch} \cong 2(\delta_1 + \delta_2) \tag{3.10}$$

The mismatch in the passive elements translates directly into a non zero common mode gain value which is in the order of the mismatch error or tolerance of the passive elements (e.g a mismatch of 1% leads to a common mode gain around -34 dB). Furthermore, since C2 must be much smaller than C1, in order to set a reasonably high closed loop gain (C1/C2), and as matching improves with size, at least matching

[4]The actual value of both capacitors of nominal value C1 are in the range $[1-\delta_1, 1+\delta_1].C1$, with $\delta_1 \ll 1$. We could consider δ_1 equal to the 3σ value of the distribution of C1. In an analog way, we consider that capacitors C2 have a tolerance δ_2, with $\delta_2 \ll 1$.

of C2 will not be optimal. On the other hand, in a OTA structure, the common mode gain is reduced by the two factors mentioned before, and can be further reduced from the values imposed by mismatch by increasing the r_{tail}.

3.2.4 Noise

It can be proved that the thermal noise input-referred power spectral density S_{ni}^{total} for the circuit shown in Fig. 3.2 is[5] (see demonstration in Appendix C):

$$S_{ni}^{total} \cong \frac{2\gamma_{si} n_N kT}{G_{m1}} \left(\frac{\gamma_{wi} n_P}{\gamma_{si} n_N} + \frac{(g_m/I_D)_{CM1}}{(g_m/I_D)_1} + \frac{I_{D2}}{I_{D1}} \Gamma \right) \tag{3.11}$$

where $(g_m/I_D)_1$ and $(g_m/I_D)_{CM1}$ are respectively the transconductance to dc drain current ratio of the input transistors of Gm1 (M1 and M2) and of the current mirror transistors of Gm1 (M3 and M4). $\gamma_{wi} = 2$ and $\gamma_{si} = 8/3$ are the excess noise factor in weak and strong inversion, respectively. n is the slope factor (the subscript indicates whether it is an NMOS or PMOS transistor), k is the Boltzmann constant, T is the absolute temperature, and Γ is:

$$\Gamma = \frac{(g_m/I_D)_2}{(g_m/I_D)_1} \frac{n_N}{n_P K_{G_{m2}}^2} + \frac{(g_m/I_D)_{CM2N}}{(g_m/I_D)_1 K_{G_{m2}}^2} + \\ + \frac{(g_m/I_D)_{CM2N}}{(g_m/I_D)_1 K_{G_{m2}}} + \frac{(g_m/I_D)_{CM2P}}{(g_m/I_D)_1} \frac{n_N}{n_P K_{G_{m2}}} \tag{3.12}$$

where $(g_m/I_D)_2$ and $(g_m/I_D)_{CM2i}$ are respectively the transconductance to dc drain current ratio of the input transistors of Gm2 (M9 and M10) and of the current mirror transistors of Gm2 (the subscript indicates whether it is an NMOS or PMOS transistor), and $K_{G_{m2}} = g_{m2}/G_{m2}$. These equations show the contribution of $K_{G_{m2}}$ in the noise reduction.

In order to reduce noise, according to Eq. 3.11, M1 and M2 have to be biased in weak inversion (maximum (g_m/I_D)), and M3 and M4 in strong inversion (low (g_m/I_D)). In order to further reduce noise it can be shown that the input transistors of Gm2 have to be biased in weak inversion and the Gm2 mirror transistors in strong inversion.

3.2.5 Design flow and design trade-offs

In this section a basic design flow for the proposed architecture, including the main design trade-offs is presented.

I_{D1} is set through the power consumption specification or the noise specification (by means of the NEF). Then, G_{m1} is set aiming to maximize $(g_m/I_D)_1$ in order to minimize noise (see Section 3.2.4) while having an acceptable size for M1 and M2. Next, by means of Eq. 3.4 and the gain specification, G_{m2} is fixed. Therefore, given the $f_{low-pass}$ specification, according to Eq. 3.3, C_L is determined.

The inversion level of the input transistors of Gm2 (related to $(g_m/I_D)_2$) has to be chosen considering the following trade-off. Firstly, $(g_m/I_D)_2$ has to be maximum in order to minimize noise (see Section 3.2.4) and power consumption. Secondly,

[5] Notation about the transconductance to dc drain current ratio: when we state $(g_m/I_D)_{ab}$, b will be 1, 2 or f, corresponding respectively to Gm1, Gm2 o Gmf. If a is omitted the transconductance to dc drain current ratio refers to the transistors of the input pair, if a is CM it corresponds to the current mirror transistors, and if it is C to the cascode transistors.

$(g_m/I_D)_2$ has to be minimum to maximize the linear range of the Gm2 input differential pair, which must be high enough to handle the maximum expected output amplitude (around $300mV_{pp}$ in this work). This trade-off is later quantified in Section 3.3 (see Fig. 3.5). On the other hand, $K_{G_{m2}}$ can be used to lower noise (the higher $K_{G_{m2}}$ the better, see Section 3.2.4) at the cost of increasing the power consumption (the higher the value of $K_{G_{m2}}$, the higher the power consumption). Once $(g_m/I_D)_2$ and $K_{G_{m2}}$ are determined, as G_{m2} was already set, I_{D2} is also determined.

The inversion level of the cascode transistors of Gm1 (M7 and M8, and therefore M6 and M5) have to be chosen considering the following aspects. On one hand, in order to achieve a very low value of $f_{high-pass}$ (see Eq. 3.5), g_{m6} and g_{m5} have to take the lowest possible value, therefore, for a given current, M6, M7, M8 and M5 have to be biased in strong inversion. On the other hand, biasing these transistors in strong inversion may lead to a high saturation voltage V_{Dsat}. Finally, another important point in order to size these transistors is the condition shown in Section 3.2.1: $g_{m7} \gg g_{m6}$ and $g_{m8} \gg g_{m5}$ where $g_{m7} \cong g_{m8}$.

Since noise contribution and power consumption of Gm2 cascode transistors are negligible, the only aspect to be considered in its design is the output swing. Then, in order to minimize the saturation voltage V_{Dsat} of these transistors, they have to be biased in weak inversion.

To determine $(g_m/I_D)_{CM1}$ (corresponding to Gm1 current mirror transistors M3 and M4) and $(g_m/I_D)_{CM2}$ (corresponding to Gm2 current mirror transistors) two elements have to be considered. Firstly, in Section 3.2.4 it was shown that from the point of view of noise reduction these transistors have to be biased in strong inversion. Secondly, low values of g_m/I_D may lead to a high value of the V_{Dsat} saturation voltage that impacts in the output swing.

M1 and M2 (Gm1 input differential pair) need to be large in order to operate in weak inversion, and hence will present very good matching and low ϵ_d error. Additionally, M3 and M4 have to operate in strong inversion with also large size (large L for small W/L), both conditions lead to low mismatch error (ϵ_{cm}). Therefore, it is possible to reduce noise and increase CMRR, at the cost of increasing the area.

Once g_{m2}, g_{m6} and g_{m5} are set, and considering that the value of C_F is bounded by the maximum value reachable within a reasonable area, and given a $f_{high-pass}$ specification, according to Eq. 3.5 G_{mf} is determined. The inversion level of the Gmf input transistors (defined by $(g_m/I_D)_f$) has to be selected paying attention to the following. On one hand, a very low $f_{high-pass}$ implies a very low value of G_{mf}, which in turn implies a low value of the W/L ratio of the Gmf input transistors. For this reason and for maximizing the linear range of the Gmf input differential pair, $(g_m/I_D)_f$ has to be minimum (strong inversion). On the other hand, biasing the Gmf input differential pair in strong inversion may lead to excessively long transistors, which may in turn result in very high values of the gate-source capacitance which impacts the load capacitance of Gm1 and hence the low-pass frequency. Therefore, biasing in moderate or weak inversion may be necessary. Finally, although from the point of view of power consumption, it might seem that the input transistors of Gmf should be biased in weak inversion, the contribution of the consumption of this stage to the overall consumption is negligible due to the low transconductance required. Once $(g_m/I_D)_f$ is established, I_{Df} is set. Finally, noise contribution and power consumption of Gmf mirror transistors are negligible, therefore a standard design can be adopted where it has to be considered the output swing and the offset.

The actual implementation resulting from these trade-offs is presented in the next section.

3.3 Implementation

A neural preamplifier based on the previously presented architecture was implemented in a 0.5 μm standard CMOS process. We designed the preamplifier according to the following specifications:

- Band-pass gain of $G = 50$ dB.
- Low-pass frequency $f_{low-pass} = 10$ kHz with an integrated $C_L = 5$ pF.
- High-pass frequency $f_{high-pass} = 18$ Hz with an integrated capacitor $C_F = 47$ pF, and $f_{high-pass} = 0.1$ Hz with an external capacitor $C_F = 10$ nF. Both integrated C_L and C_F were built as poly−poly capacitors for maximum linearity.
- CMRR greater than 80 dB.
- Input-referred around 2 μV_{rms}.
- NEF around 2.

In order to obtain a NEF around 2, $I_{D1} = 3.75$ μA was taken. The Gm1 mirrors (M3 and M4) were biased[6] in deep strong inversion taking $(g_m/I_D)_{CM1} = 2.5$ V^{-1}, which implies a $V_{Dsat} = 590$ mV. The transistors of the Gm1 input differential pair (M1 and M2) were biased in deep weak inversion with a $(g_m/I_D)_1 = 27$ V^{-1}. In order to assess the impact on flicker noise, taking an almost minimum M1 and M2 transistor length $L_1 = 1$ μm, different cases were simulated varying the M1 and M2 transistor width W_1. Table 3.1 and Table 3.2 show the noise performance for the main values of the $(W/L)_1$ considered. The noise integration bandwidth considered in these simulations ranges from 3.2 nHz to 100 MHz. As expected, the higher W_1 the lower the contribution of the flicker noise. Finally, $W_1 = 8000$ μm and $L_1 = 1$ μm were chosen.

Table 3.1: Schematic simulations of noise performance for different values of W/L ratio of the Gm1 input differential pair, with $f_{high-pass} = 18$ Hz (fully-integrated capacitors).

$(W/L)_1$ (μm)	2000/1	4000/1	8000/1	12000/1
M1/M2 area (μm^2)	2000	4000	8000	12000
g_{m1} (μS)	94.0	98.0	101.0	102.5
$(g_m/I_D)_1$ (V^{-1})	25.7	26.7	27.5	27.9
Gain (V/V)	288	299	306	309
v_{ni} (μV_{rms})	2.23	2.11	2.05	2.02
NEF	2.33	2.20	2.14	2.11

A comparison between Table 3.1 and Table 3.2 shows that it does not make a big difference, regarding noise performance, to vary the high-pass frequency between 0.1 Hz and 18 Hz. This happens because the thermal noise is integrated through a wide bandwidth (10 kHz) making the flicker noise generated between 0.1 Hz and 18 Hz negligible. The same behavior is reported in [57].

In order to make the loss of gain negligible, α was set to 100[7], assuring that $g_{m7} \gg g_{m6}$ and $g_{m8} \gg g_{m5}$ due to $g_{m7}/100 = g_{m6}$ and $g_{m8}/100 = g_{m5}$.

[6] Throughout the text g_m/I_D values are reported at room temperature.

[7] $\alpha = 100$ was chosen as an arbitrarily large number, that was then verified that lead to good results. Low values of alpha reduce the gain and allow the circuit to block higher levels of dc input signals. On the other hand, high values of alpha increase the gain and decrease the dc input block capacity. In addition, low values of alpha reduce the output resistance of Gm1, which in turn impacts in the overall OTA performance.

Table 3.2: Schematic simulations of noise performance for different values of W/L of the Gm1 input differential pair, with $f_{high-pass}$ = 0.1 Hz (external capacitor C_F).

$(W/L)_1$ (μm)	4000/1	8000/1
M1/M2 area (μm^2)	4000	8000
g_{m1} (μS)	97.8	100.8
$(g_m/I_D)_1$ (V^{-1})	26.7	27.5
Gain (V/V)	295	306
v_{ni} (μV_{rms})	2.20	2.08
NEF	2.30	2.17

Fig. 3.5 introduces the Gm2 linearity noise current-consumption trade-off (previously mentioned in Section 3.2.5) and shows how $(g_m/I_D)_2$ is a useful tool to evaluate this trade-off. The figure presents the noise contribution of Gm2 (which is the third term of Eq. 3.11), the current consumption of Gm2 and its input linear range (taken from [104, Eq. 9] with a linearity error of 10%). In our case, $(g_m/I_D)_2$ = 9.3 V^{-1} was set (this allows an input linear range of 300 mV_{pp}). Additionally, $(g_m/I_D)_{CM2N} = (g_m/I_D)_{CM2P}$ = 4.5 V^{-1} was taken.

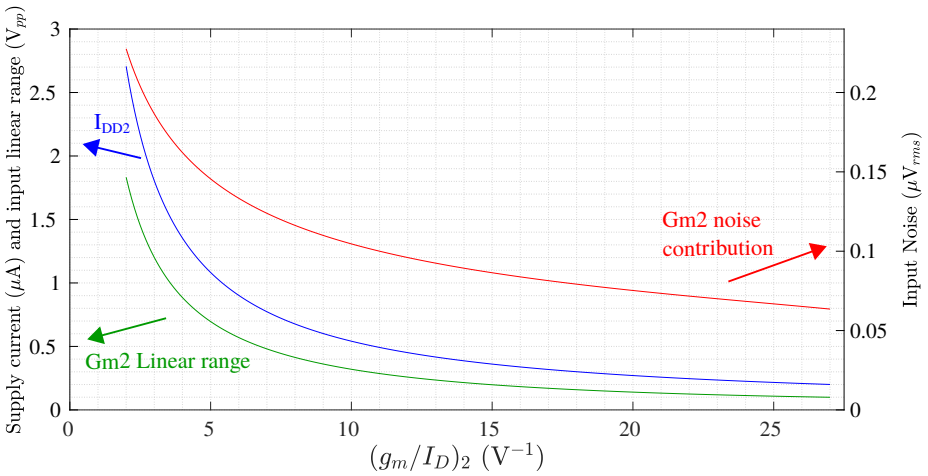


Figure 3.5: Gm2 linearity noise current-consumption trade-off.

In order to achieve a very low high-pass frequency within a reasonable area and without an external capacitor, the lowest possible value for G_{mf} has to be taken. To have a G_{mf} around 1 nS the technique proposed in [105] that divides the current using series-parallel current mirrors was used. The current division factor implemented was $K_{G_{mf}}$ = 72.5, establishing a $f_{high-pass}$ = 18Hz with an integrated capacitor C_F = 47pF, and a $f_{high-pass}$ = 0.1 Hz with an external capacitor C_F = 10nF. The same technique was used in Gm2 with a current division factor of $K_{G_{m2}}$ = 8.5 (in this case for noise reduction).

According to what was discussed in Section 3.2.3 and Section 3.2.5, two techniques were implemented to guarantee a high CMRR. Firstly, as mentioned before, large M1, M2, M3 and M4 transistors were adopted, thus improving matching. Secondly, the r_{tail} of the current source of Gm1 was increased by cascoding it. To bias the cascode transistor the technique proposed in [106] was used. This allows to generate the bias voltage in such a way that the transistor of the current mirror operates in weak

inversion and its V_{DS} is just a little higher than V_{Dsat}. This is done by means of a single diode connected transistor, avoiding the need of using a dc voltage source and eventually an external pin. Although this technique was very useful, our design did not pay enough attention to the consumption nor the area of this auxiliary circuit, resulting in occupying an important area and a current consumption not negligible[8].

The power supplies were set in $V_{DD} = 1.65$ V and $V_{SS} = -1.65$ V. The dc gate voltage of M7 and M8 and the reference values of Gm2 and Gmf were set in $(V_{DD} + V_{SS})/2 = 0$ V. This 0 V voltage, the mid-point between the supply voltages, is hereinafter referred to as "ground", and the output is referred to this voltage. The common-mode voltage of the gates of M1 and M2 has to be higher than ground, so it was set to 0.6 V, this voltage is hereinafter referred to as "REF".

According to the aforementioned considerations a neural preamplifier was fabricated in a 0.5 μm standard CMOS process (see Fig. 3.6). The area was not optimized. While the core of the preamplifier occupies 0.335 mm^2 (including capacitors), biasing and testing circuits occupy 0.322 mm^2. The area of the biasing and testing circuits could be much reduced. The distribution of the area is as follows: $A_{Gm1} = 0.219\ mm^2$ (65.37%), $A_{Gmf} = 0.040\ mm^2$ (11.94%), $A_{Gm2} = 0.021\ mm^2$ (6.27%), $A_{C_F} = 0.048\ mm^2$ (14.33%) and $A_{C_L} = 0.007\ mm^2$ (2.09%).

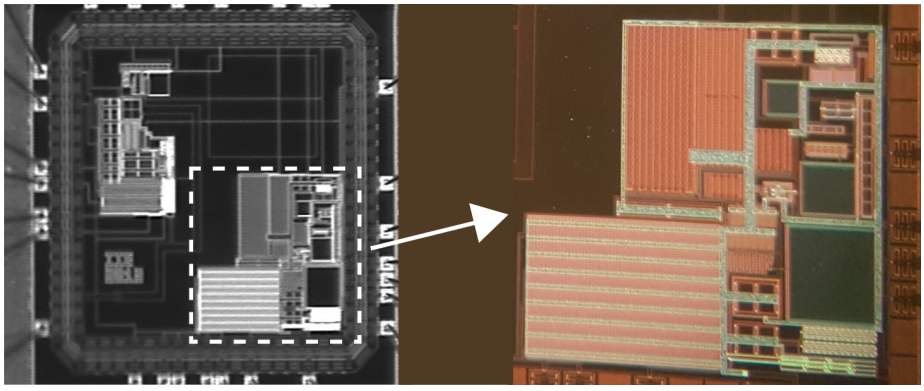


Figure 3.6: Microphotograph of chip containing a preamplifier with the proposed architecture (dashed white rectangle). The area of the preamplifier core is 0.335 mm^2 (including capacitors).

The main parameters of the preamplifier are presented in Table 3.3.

3.4 Experimental results

3.4.1 Testbench results

This Section presents results of the laboratory characterization of two samples of the same chip (named IC#01 and IC#02) and post-layout simulations. The samples were randomly selected from the received prototype chips. The consistency between the results of the two samples, and the simulations including 500-runs MC mismatch ones was deemed enough to confirm the expected performance of the chip. I_{DD} is the total current consumption of the preamplifier, v_{ni} is the input-referred noise voltage, PSD

[8]This circuit has two branches that each consumes $I_{BIASGm1}/10$ which represents 1.54 μA and will not be considered in the following sections as part of the preamplifier consumption, because the consumption of these branches can be adjusted to $I_{BIASGm1}/100$ and make it negligible.

Table 3.3: Preamplifier main parameters (post-layout simulations).

	Gm1	Gm2	Gmf
$(g_m/I_D)_{InDifPair}$	27.5 V^{-1}	9.3 V^{-1}	17.1 V^{-1}
$(g_m)_{InDifPair}$	101 μS	2.7 μS	86 nS
G_m	100 μS	320 nS	1.2 nS
$(I_D)_{InDifPair}$	3.67 μA	291 nA	5 nA
$(W/L)_{InDifPair}$	7776/1.05	3.3/6	3/42
K_{G_m}	1.0	8.5	72.5
$(g_m/I_D)_{CM}$	2.5 V^{-1}	4.5 V^{-1}	-
g_{m6}	735 nS	-	-
g_{m5}	710 nS	-	-
g_{m7}	91 μS	-	-
g_{m8}	83 μS	-	-

corresponds to the noise power spectral density, PSRR+ is the positive power supply rejection ratio (V_{DD}), PSRR- refers to the negative power supply rejection ratio (V_{SS}), ICMR is the input common-mode range and "Output Offset" is the output dc voltage deviation from ground. To measure Gain and CMRR we used input signals of 1 mV_{pp} and 100 mV_{pp} respectively. PSRR+ and PSRR- were measured by introducing a signal of 100 mV_{pp} and 50 Hz in the respective supply source. The simulation values correspond to the typical values unless otherwise indicated.

Table 3.4 summarizes the main characteristics of the proposed preamplifier. In general terms, expected theoretical values and simulation results agree with measured data in both chips. However, PSRR- with fully-integrated capacitors is lower than expected. This is because the integrated $C_F = 47pF$ was connected by mistake to V_{SS} instead of ground. The proposed architecture is very competitive with other amplifiers in the state-of-the-art as will be shown in Section 3.4.3.

Table 3.4: Preamplifier main characteristics. Experimental results from two chips (IC#01 and IC#02) with fully-integrated capacitors and external capacitor C_F = 10 nF.

	Simulation		IC#01		IC#02	
	Fully-int	Ext. C_F	Fully-int	Ext. C_F	Fully-int	Ext. C_F
Gain (dB)	49.7	49.6	49.6	49.2	49.5	49.3
$f_{high-pass}$ (Hz)	17.9	0.1	13.0	0.1	12.0	0.1
$f_{low-pass}$ (kHz)	9.6	9.6	9.8	10.3	9.7	10.6
I_{DD} (μA)	8.10	8.10	8.48	8.45	8.41	8.49
v_{ni} (μVrms)*	1.92	1.96	1.88	1.94	2.03	2.07
NEF	2.15	2.19	2.13	2.14	2.30	2.25
Noise integration bandwidth (Hz)	3.2n-100M		0.03-25k		0.03-25k	
CMRR @ 1kHz (dB)*	89.7	90.9	87.0	87.6	92.0	91.6
PSRR+ @ 50Hz (dB)*	73.7	82.1	74.9	72.4	76.9	86.4
PSRR- @ 50Hz (dB)*	35.2	68.1	35.1	63.2	35.0	67.1
Output Offset (mV)*	2.0±11.6	2.0±12.0	-1.4	-8.3	8.1	-3.0

* the simulation value corresponds to the mean value of the 500-runs MC simulation, otherwise the typical value is reported.

Fig. 3.7 shows the measured and simulated frequency response for two cases,

fully-integrated capacitors and external C_F capacitor. In Fig. 3.8 and Fig. 3.9 the simulated and measured output-referred noise PSD with fully-integrated capacitors and external C_F capacitor respectively is depicted.

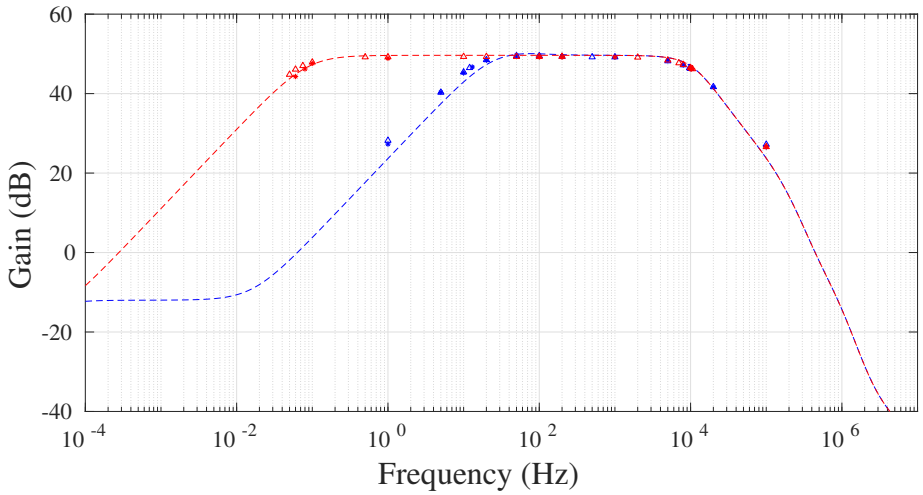


Figure 3.7: Frequency response with fully-integrated capacitors (blue) and external capacitor C_F = 10 nF (red). Measurements (IC#01 = asterisks and IC#02 = triangles) and simulations (dashed line).

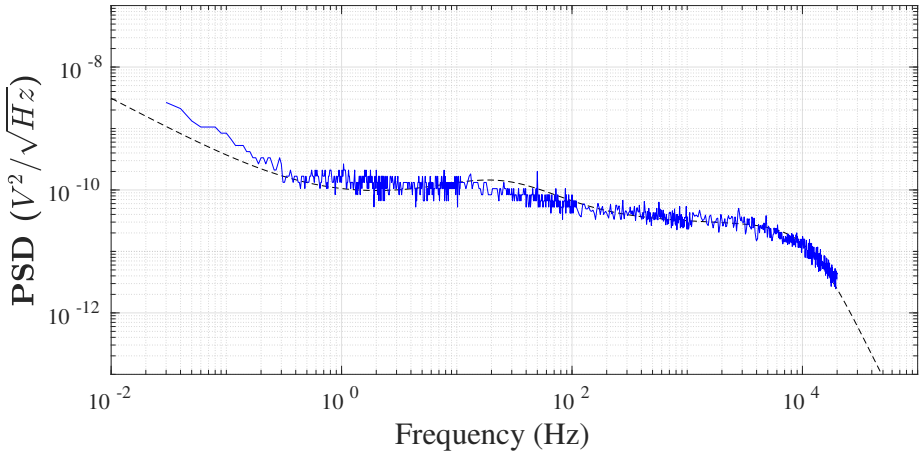


Figure 3.8: Ouput-referred noise PSD with fully-integrated capacitors. Measured at the output of IC#01 (solid blue) and simulated (dashed black). Integration under the solid curve divided by gain G yields to an input-referred noise voltage of 1.88 μV_{rms}.

Fig. 3.10 shows the measured and simulated CMRR for the fully-integrated capacitors version. The performance in terms of CMRR is outstanding: below 4 kHz is always greater than 80 dB, at this frequency it starts to fall, but at 10 kHz it is still greater than 70 dB. In addition, at 50 Hz the measured value is 90.3 dB, and the 500 runs MC simulation worst-case and best-case are respectively, 81.8 dB and 123.3 dB.

As it was stated in Section 3.2.2 the gain is the only parameter affected by the dc

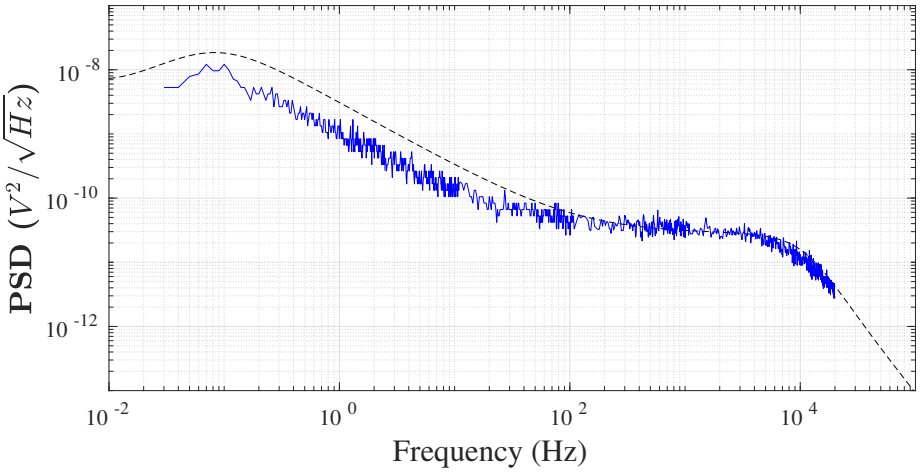


Figure 3.9: Output-referred noise PSD with external capacitor C_F = 10 nF. Measured at the output of IC#01 (solid blue) and simulated (dashed black). Integration under the solid curve divided by gain G yields to an input-referred noise voltage of 1.94 μV_{rms}.

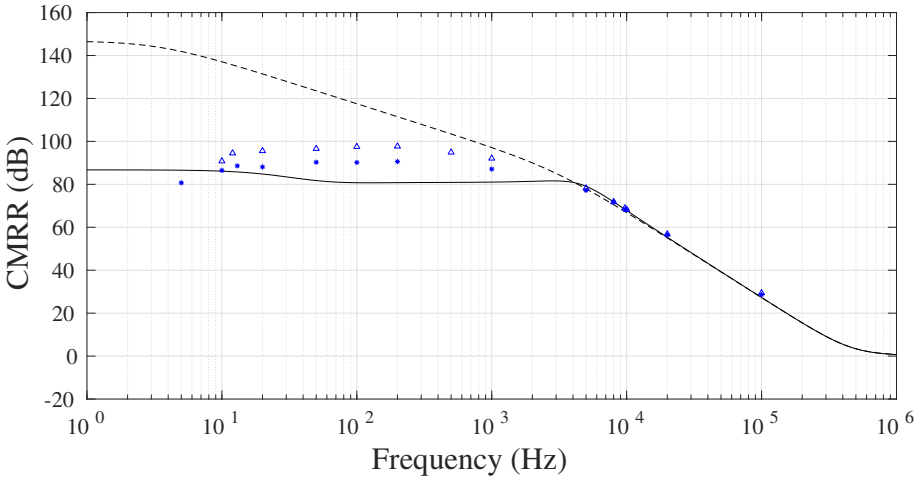


Figure 3.10: Common-mode rejection ratio (CMRR) with fully-integrated capacitors. Measurements (IC#01 = blue asterisks and IC#02 = blue triangles) and 500 runs MC simulations (black lines). The best-case iteration of MC simulation is depicted in dashed black line, and the worst-case iteration in solid black line.

blocking technique proposed in our architecture. In Table 3.5 gain measurements for different input dc voltages $V_{IN,dc}$ are presented. There it can be seen that the loss of gain is admissible for input dc voltages lower than 50 mV. As discussed in Section 2.3, our result is more than acceptable since the undesired input dc signals are typically in the range of 1 mV - 10 mV, and can be up to a maximum of 50mV [56]. In addition, in many applications, small variations in the amplitude are not significant (e.g. spikes detection).

The preamplifier ICMR is 380 mV (within a ±1.65 V power supply). This value of ICMR assures a loss of gain lower than 0.5 dB and a CMRR greater than 80 dB

Table 3.5: Dc blocking capacity with fully-integrated capacitors and external capacitor $C_F = 10$ nF. Gain simulations and measurements for different dc voltage inputs $V_{IN,dc}$. These measurements were performed at 1 kHz.

	Simulation		IC#01		IC#02	
$V_{IN,dc}$	Fully-int	Ext. C_F	Fully-int	Ext. C_F	Fully-int	Ext. C_F
0 mV	49.7 dB	49.6 dB	49.5 dB	49.2 dB	49.5 dB	49.3 dB
50 mV	41.4 dB	41.4 dB	41.9 dB	40.7 dB	40.3 dB	40.6 dB
100 mV	31.8 dB	31.7 dB	29.7 dB	30.8 dB	29.8 dB	30.3 dB

(see Fig. 3.11). This ICMR is more than enough to accommodate typical common-mode signals. The Gain and CMRR measurements were performed in the band-pass (200 Hz) with fully-integrated capacitors. Fig. 3.11 shows that, in order to guarantee a loss of gain lower than 0.5 dB and a CMRR greater than 80 dB, the preamplifier inputs need to be biased to a common-mode potential (REF) in the range from 0.32 V to 0.70 V being 0 V the mid-point between the supply voltages. This can be easily implemented, as will be shown in the application example presented in Subsection 3.4.2 (see Fig. 3.15).

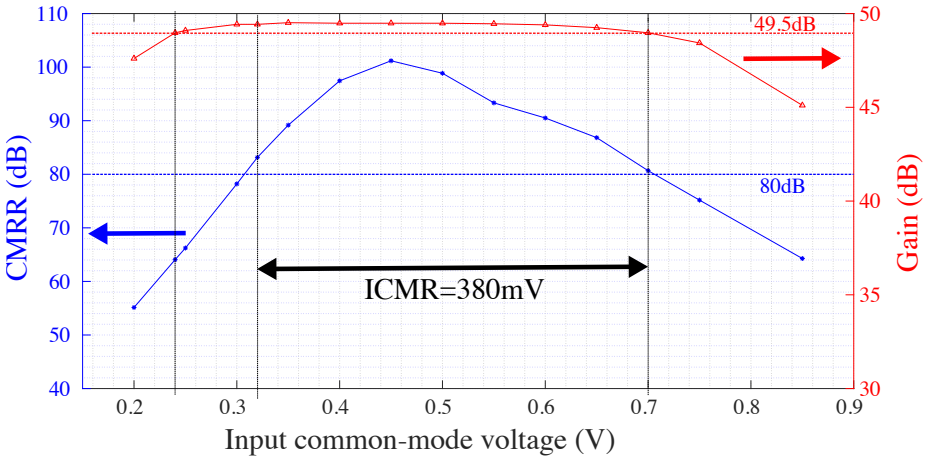


Figure 3.11: ICMR measurement with fully-integrated capacitors. IC#01 Gain (red) and CMRR (blue) measurements for different dc input common-mode voltages (referred to ground). The figure shows that the ICMR is 380 mV (with a ±1.65 V power supply). These measurements were performed at 200 Hz.

Figures 3.12 and 3.13 present results of PSRR+ and PSRR- with fully-integrated capacitors respectively. PSRR+ is adequate for the targeted applications. However, as previously mentioned, PSRR- resulted in a lower value than expected. This is because the integrated $C_F = 47$ pF was connected by mistake to V_{SS} instead of ground.

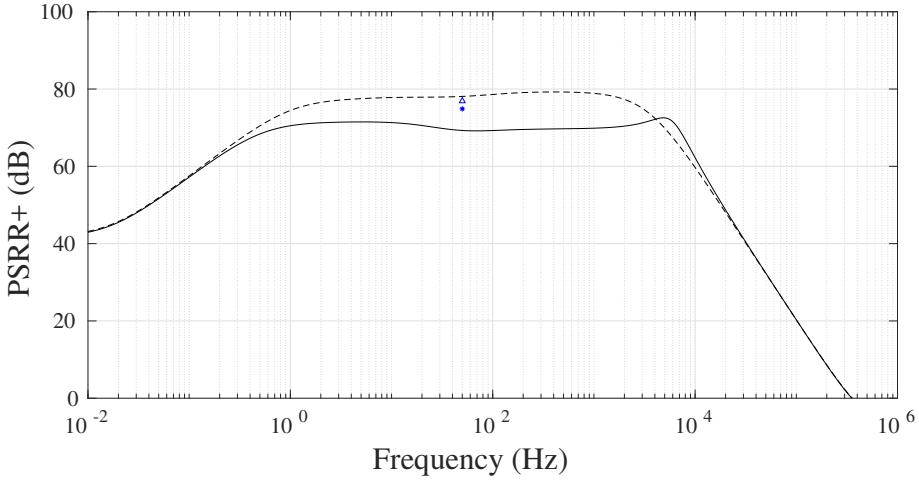


Figure 3.12: Positive power supply rejection ratio (PSRR+) with fully-integrated capacitors. Measurements (IC#01 = blue asterisk and IC#02 = blue triangle) and simulations (black lines). The best-case iteration of MC simulation is depicted in dashed black line, and the worst-case iteration in continuous black line.

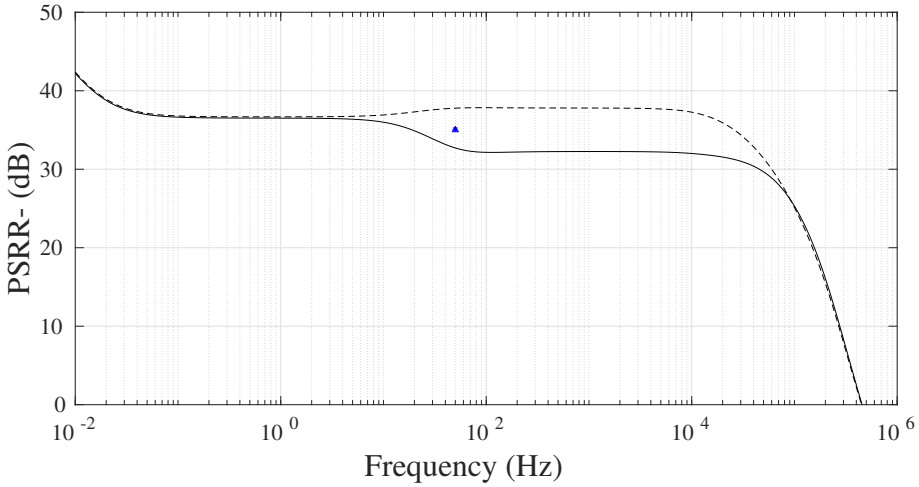


Figure 3.13: Negative power supply rejection ratio (PSRR-) with fully-integrated capacitors. Measurements (IC#01 = blue asterisk and IC#02 = blue triangle) and simulations (black lines). The best-case iteration of MC simulation is depicted in dashed black line, and the worst-case iteration in continuous black line.

3.4.2 Weakly electric fish in-vivo recording

Our preamplifier has proved to be highly appropriate for in-vivo recording of LFPs and unitary signals from the brain stem of weakly electric fish *Gymnotus omarorum*.

Two in-vivo experiments were performed for testing our preamplifier. Firstly, a freely-moving fish experiment with a pair of thin wires (60 μm diameter, insulated except at the tip), attached to the skull with dental cement, chronically-implanted at the mesencephalon (see Fig. 3.14). Secondly, an acute experiment with the fish still, consisted in a multitrode (Michigan type) inserted in the electrosensory lobe (one recording spot was connected to the preamplifier positive input and a copper wire of 80 μm diameter insulated except at the tip was connected to the negative input).

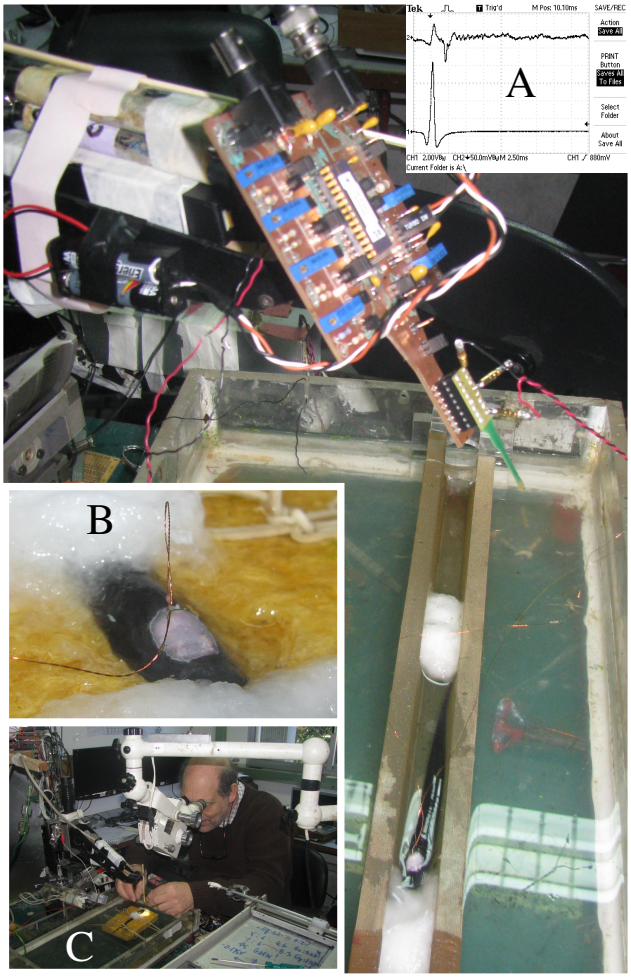


Figure 3.14: In-vivo recording setup (freely-moving fish experiment). Main figure shows a fish chronically implanted at the mesencephalon with a pair of thin wires (60 μm diameter, insulated except at the tip). The fish can swim in a mesh pen. Above the fish, an unshielded custom PCB supporting our integrated preamplifier is shown. Inset panel A: fast field potential recorded in the freely-moving fish (up), and EOD recorded in the water (down). Inset panel B: close up of the fish's head showing the fixation of the wires to the skull with dental cement. Inset panel C: surgical implantation of the freely-moving fish.

In both experiments, the aforementioned electrodes were simultaneously connected to an unshielded custom Printed Circuit Board (PCB) supporting our preamplifier and to a standard shielded biopotential instrumentation system *Microelectrode AC Amplifier 1800* from *A-M Systems*. This amplifier features a CMRR greater than 80 dB, an input-referred noise of 3 μV_{rms} (10 Hz - 100 kHz), gain and bandwidth are programmable, and it is powered from the mains. Despite the fact that the Microelectrode AC amplifier 1800 was not designed to perform recordings in freely-moving fish (mainly because of its size and the fact that it is powered from the mains), we were able to record simultaneously with both amplifiers, but fish movements were restricted in order to protect the animal. The output of both amplifiers were sampled through a *Datawave Technologies* acquisition system.

The experimental setup is shown in Figs. 3.15 and 3.14. A third wire placed at the dorsal muscle mass acted as a common-mode reference for both amplifiers (named REF in Fig. 3.15). The ground of our amplifier is referred to the fish (and to the rest of the acquisition system) by means of an auxiliary circuit formed by $R_1 = 470\Omega$, $R_2 = 2.2\ k\Omega$ and $C_1 = 100$ nF // 47 μF (shown in Fig. 3.15). This circuit sets the middle point of our amplifier power supplies to a specific and configurable voltage below REF. According to what was discussed in Subsection 3.4.1, REF needs to be biased to a common-mode potential in the range from 0.32 V to 0.70 V being 0 V the mid-point between the supply voltages. In other words, the ground of our amplifier needs to be biased to a potential in the range from -0.32 V to -0.70 V (referred to REF). In these experiments the ground of our amplifier was set in -0.6 V from REF.

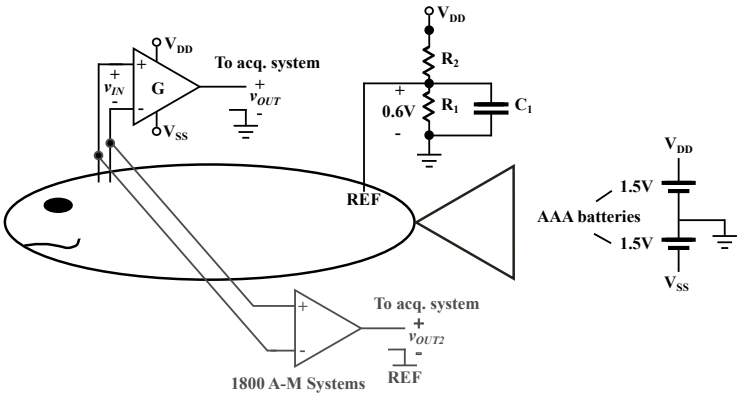


Figure 3.15: In-vivo recording setup (still and freely-moving fish experiments). Electrodes were simultaneously connected to our preamplifier (powered by 2 AAA batteries) and to a standard instrumentation system (*Microelectrode AC Amplifier 1800* from *A-M Systems*) powered from the mains. The output of both amplifiers were sampled through a *Datawave Technologies* acquisition system. A third electrode (REF) placed at the dorsal muscle mass acted as a common-mode reference for both amplifiers.

Fig. 3.16 shows the effect of the EOD at the output of the preamplifier, where it can be seen that the EOD is firing every 90 ms approximately. Note in this figure the perfect matching of the signals recorded with our unshielded low-power amplifier (solid line) with those recorded with the shielded ac-plugged commercially available amplifier (dashed line). Fig. 3.16 and Fig. 3.14-A display in detail the EOD artifact and a short-latency fast LFP recorded in the acute and chronically implanted fish respectively.

In Fig. 3.16 two phenomena can be observed. Firstly, the input signal common mode voltage (mainly due to the EOD) is largely attenuated. Secondly, due to unbal-

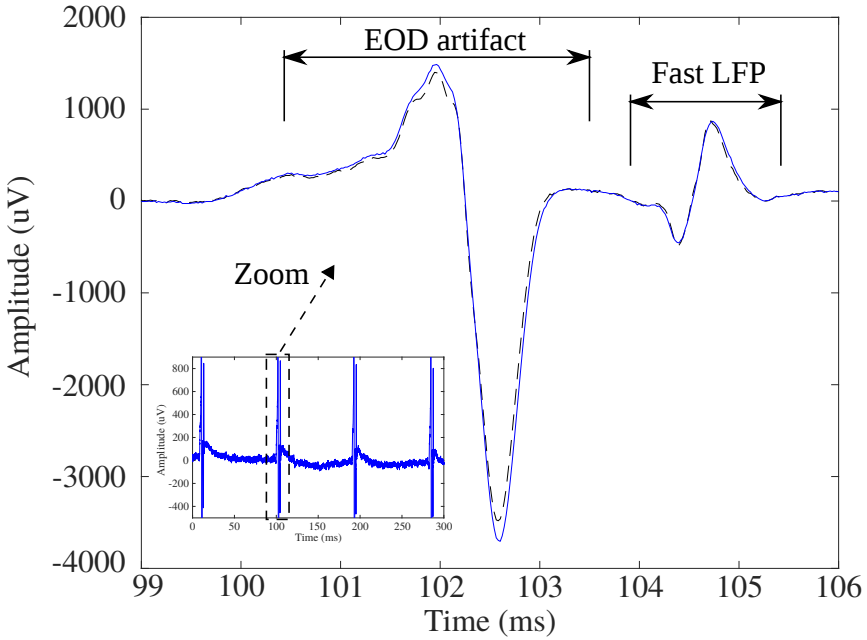


Figure 3.16: In-vivo recording of a weakly electric fish *Gymnotus omarorum* (still fish experiment). Fast LFP and EOD artifact are indicated. In solid blue the recording from our amplifier and in dashed black the one from the *Microelectrode AC Amplifier 1800* from *A-M Systems*. Each recorded signal is referred to the input of its corresponding amplifier (the amplitude of the output signal is divided by the amplifier gain).

ances between impedances at the tissue-electrode interface, the EOD give place to a differential mode voltage at the amplifier input (usually called "EOD artifact"), which is consequently amplified (for this reason we achieve a perfect matching in the signal recorded with our amplifier and the AM-1800 system). This conversion from common to differential mode is usually called "potential divider effect" [107].

Fig. 3.17 shows a recording from a freely-moving experiment performed with another fish. In this case the EOD is firing every 50 ms approximately. A slow LFP can be observed, as well as the Fast LFP, the EOD artifact and unitary activity. In order to simultaneously record Slow LFP and unitary activity, the preamplifier was used with external $C_F = 10$ nF.

Finally, Fig. 3.18 shows in-vivo neural unitary activity recordings obtained with our amplifier. The amplitude of the EOD measured at the inputs of the preamplifier was approximately 100 mV_{pp}. Therefore, in this particular experiment, we were able to accurately record 500 $\mu\mathrm{V}_{pp}$ spikes superposed to a 200 times higher EOD.

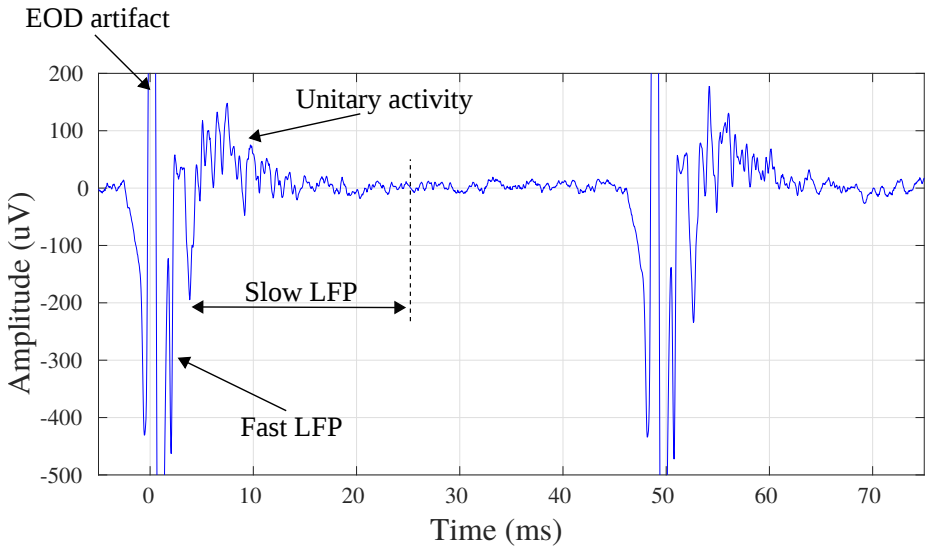


Figure 3.17: *Gymnotus omarorum* in-vivo recording (freely-moving experiment).

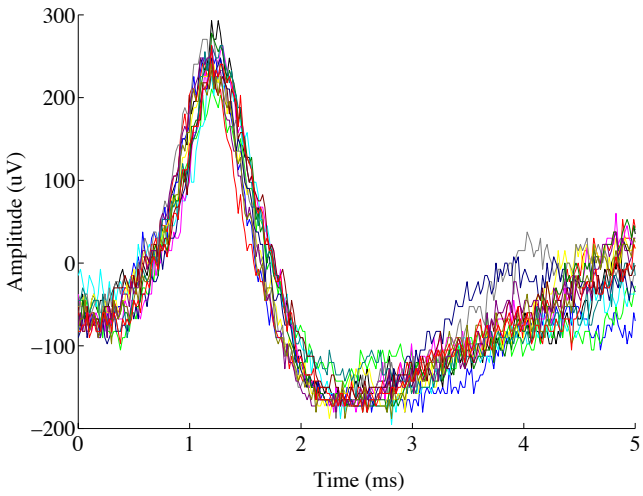


Figure 3.18: Superimposed traces of a single unit repetitively active in the electrosensory lobe corresponding to the still fish experiment. Note the similarity of the time course and the large signal to noise ratio.

3.4.3 Comparison with previous work

As discussed in Section 3.1, over the last years remarkable research work has been done in this area. Some amplifiers were selected from this rich background. Table 3.6 summarizes the main performance parameters of our preamplifier compared to state-of-the-art implementations. The rationale behind this table can be summarized as following:

1. We have prioritized works that take specially into account the CMRR [81], or report a worst-case simulation [57]. [57] is also included for historical reasons.
2. We have prioritized works that achieve outstanding results of CMRR and present a reasonable performance in NEF and input noise [64, 82]. [82] is also interesting because it does not implement the architecture of Harrison et al.
3. Residual criterion: works that present acceptable values of CMRR (greater than 60 dB) and exhibits a very good performance in current-efficiency (NEF lower than 3) and input-referred noise lower than 4 μV_{rms}.

The parameter "CMRR worst-case" corresponds to a measured or simulated worst-case value. In our preamplifier we report the worst-case value at 50 Hz in a 500-runs MC simulation.

As mentioned in Section 3.1, in order to correctly compare input noise, NEF and PEF performance, it is necessary to consider the adequate noise integration bandwidth. For this reason, the measurements where the noise integration bandwidth only covers the amplifier bandwidth were marked with (*) in Table 3.6. The actual NEF, PEF and input noise of these works, when integrated in the whole bandwidth, should be higher than the reported ones.

As mentioned in Section 2.3, PEF is strongly dependent on the supply voltage of the circuit, which in turn it is dependent on the manufacturing process and its threshold voltage. The architecture presented here shows a similar or even a much better PEF than other circuits manufactured in similar processes, like [57, 61, 63, 68, 69, 82]. For instance, despite that this kind of extrapolation is not straightforward, if our V_{DD} is scaled in a process with smaller channel length and threshold voltage, the resulting PEF value gets closer to the best figures shown, or even better than the other preamplifiers that provide high CMRR (our PEF would scale to 5.3 if the circuit is powered with a 1.2 V supply voltage in a 0.18 μm or smaller process). Another aspect directly related to the manufacturing process is the resulting area. This should be taken into account when comparing this characteristic of the design. In the framework of an undergraduate thesis [108], a first approach to implement our architecture in a 130 nm process was done (this topic will be taken up in Chapter 7).

Some existing works [64, 82] present an excellent value of CMRR (greater or equal to 90 dB), however they do not include a worst case or spread analysis that allows to assess the full CMRR performance in face of mismatches. Furthermore, these CMRR values are not achieved jointly with low NEF or low input noise. Table 3.6 shows that our work performs well in line with other state-of-the-art neural preamplifiers. Indeed, our work is the best choice for applications that simultaneously seek low noise, high CMRR and current-efficiency.

Table 3.6: Comparison with prior work.

	JSSC '03 [57]	TBCAS '07 [61]	TBCAS '12 [47]	ESSCIRC '10 [63]	TNSRE '09 [64]	TBCAS '13 [65]	TCAS-I '13 [66]	TBCAS '14 [68]	TBCAS '17 [69]	TCAS-I '16 [81]	JETCAS '11 [82]	This work fully-int.	This work ext. C_F
Technology (μm)	1.5	0.5	0.13	0.35	0.35	0.18	0.18	0.35	0.35	0.065	0.35	0.5	0.5
Gain (dB)	39.5	40.8	47.5	65	40	52.0	40.0	40.8	46	52.1	46.0	49.5	49.2
$f_{low-pass}$ (kHz)	7.2	5.3	6.9	10.5	20	10.0	5.1	10.0	8.3	8.2	10.0	9.8	10.3
$f_{high-pass}$ (Hz)	25m	45	167	300	0.1	0.25	0.38	0.1	0.05	1.0	200	13.0	0.1
Supply current (μA)	16.0	2.7	1.6	4.3	2.0	1.6	0.8	4.3	3.2	3.3	22.4	8.5	8.5
Input noise (μV_{rms})	2.2	3.06	3.8	3.05	4.9 (*)	3.2 (*)	4.0 (*)	2.8	3.86	4.13 (*)	2.9	1.88	1.94
NEF	4.0	2.67	2.26	2.5	1.92 (*)	1.57 (*)	1.93 (*)	2.25	2.8	3.19 (*)	6.6	2.13	2.14
Noise integration bandwidth (Hz)	0.5-50k	10-98k	1-100k	0.5-50k	0.1-20k	1-10k	1-8k	0.05-200k	N/A	1-8.2k	N/A	0.03-25k	0.03-25k
$CMRR_{worst\text{-}case}$ (dB)	42	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	46	N/A	82	84
$CMRR_{measured}$ (dB)	83	66	83	65	90	73	60	70	69	80	110	87	88
PSRR (dB)	85	75	70	50	80	80	70	70	72	78	110	74	82
THD 1% (mV_{pp})	16.7	7.3	3.1	N/A	N/A	N/A	0.8	3.0	N/A	0.7	>20	0.7	0.7
Area (mm^2)	0.16	0.16	0.05	0.10	0.18	0.25	0.04	0.17	0.06	0.04	0.15	0.34	0.34
V_{DD} (V)	5.0	2.8	1.2	3.0	3.3	0.45	1.0	2.5	3.0	1.0	3.3	3.3	3.3
PEF	80	20.0	6.1	18.8	12.2 (*)	1.1 (*)	3.7 (*)	12.7	23.5	10.2 (*)	144	15.0	15.1

(*) Noise integration bandwidth only covers the amplifier bandwidth: actual PEF, NEF, and, input noise, when integrated in the whole bandwidth, should be higher than the reported ones

N/A = Not Available.

3.5 Safety considerations

The proposed neural recording architecture could be applied to medical devices, including implantable ones. In this scenario, the safety of the proposed circuit needs to be considered. The standards and regulations for active implantable medical devices require that the dc current leakage towards the tissue (which may damage it) to be below 1 μA [109, Cl. 16.2]. In addition, safety should be preserved even under single failure condition [109, Cl. 19.3]. In this case, the standards and regulations do not state a numerical value, but require that the failure *shall not cause an unacceptable hazard*, which depending on the application this may allow for a leakage a bit higher than 1 μA. In any case, it should be analyzed the suitability of the proposed architecture from this point of view.

In the case of the architecture of Harrison et al. the prevention of dc leakage under normal and single fault conditions is helped by the use of series input capacitors. In our case, under no failure conditions, the dc leakage is prevented by the isolation of the gate oxide of the input transistors. On the other hand, Fig. 3.19 shows the case of a single failure that short circuits the gate of one of the input transistors to its source or drain (the figure analyze M2, an analog reasoning can be conducted for M1). In both cases, the dc current I_{TISSUE} that will flow through the body, can be limited by the values of R_1 and R_2[9]. For instance, if the value of these resistors is in the order of MΩs, the value of I_{TISSUE} will be in the order of hundreds of nano-amperes, which is a safe value. The high value of these resistors does not affect the noise performance of the circuit because its thermal noise is filtered by C_1 (the noise contribution will be $\sqrt{kT/C_1}$).

The previous analysis is not intended as a complete risk and safety analysis for the proposed circuit. A complete analysis needs to be carried out in a particular system and application. It just tried to show that the proposed circuit does not entail complications regarding safety aspects related to dc leakage to the body under normal and single failure conditions as required by the regulations and standards of active implantable medical devices, which is the more demanding application case in terms of safety.

3.6 Conclusions

This work presented a novel neural preamplifier architecture, including silicon implementation and experimental characterization. This architecture was presented and analyzed in depth, with a strong focus in the technique that efficiently blocks the dc input signal and sets the high-pass frequency, deriving the preamplifier transfer function and the main design equations. This architecture enables a low noise, high CMRR and current-efficient neural preamplifier, with a high-pass frequency fixed without MOS pseudo-resistors.

A fully-integrated neural preamplifier, with an overall state-of-the-art performance and enhanced CMRR, was fabricated in a 0.5 μm CMOS process. In general terms, expected theoretical values and simulation results agree with measured data in both chips. Results from measurements show that the CMRR is greater than 87 dB, the equivalent input noise is 1.88 $\mu\mathrm{V}_{rms}$ and the NEF is 2.1. To the best of our knowledge, our amplifier is the best option for applications that simultaneously need low noise, high CMRR and current-efficiency. cdA second version of the preamplifier with one external capacitor achieves a high-pass frequency of 0.1 Hz while keeping the

[9]For a short circuit between gate and drain other current pathways can be considered. In all cases, the current will be limited by R_1 and R_2.

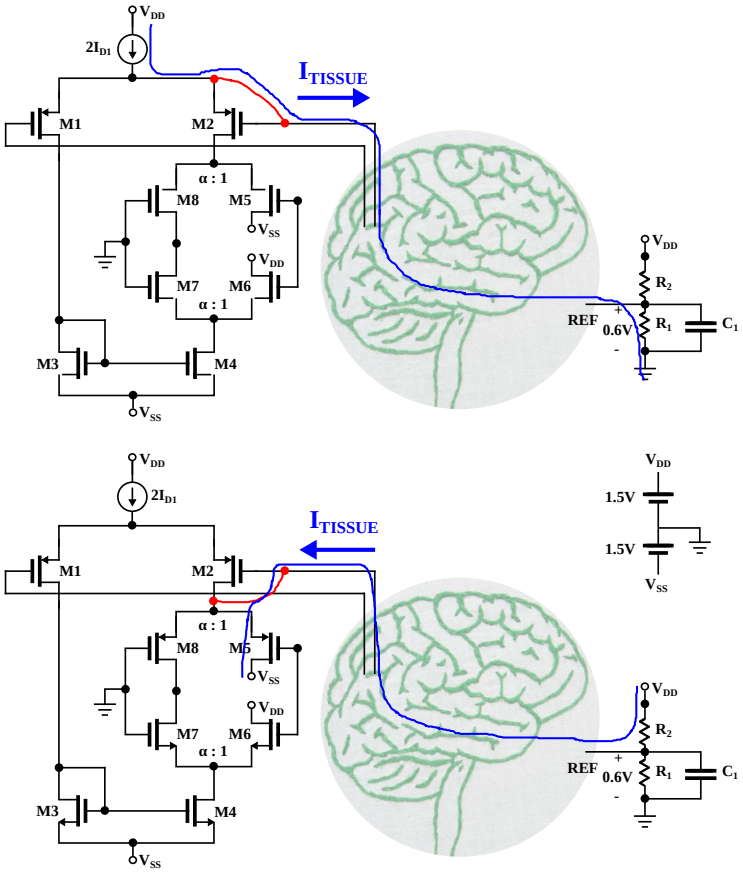


Figure 3.19: single failure safety analysis: the short circuits between the gate of M2 and its source (up) or drain (down) are marked in red. The brain depicted in the figure was taken from *Brain Embroidery* by Hey Paul Studios (licensed under CC BY 2.0).

performance of the fully-integrated version.

In addition, this work has presented in-vivo measurements made with the proposed architecture in a weakly electric fish (*Gymnotus omarorum*), showing the ability of the preamplifier to acquire neural signals from high amplitude common-mode interference in an unshielded environment. Moreover, signals recorded with our unshielded low-power battery-operated amplifier perfectly match those recorded with a shielded ac-plugged commercial laboratory instrumentation system. Finally, the proposed preamplifier has proved to be highly appropriate for in-vivo recordings of LFPs and unitary signals from the brain stem of a weakly electric fish.

Chapter 4

A novel band-pass biquad filters architecture

Second-order filters, often referred as biquads, can be configured to be universal filters and they are suitable for cascade connection in order to achieve higher order filters [110]. These filters are key blocks of AFEs and other important circuits. In this chapter we extend and apply the architecture presented in Chapter 3 to biquad band-pass filters showing the versatility of the proposed architecture. This chapter is an adapted version of [30].

Continuous-time integrated Gm-C filters, have received considerable interest in various applications, such as hard-disc drives, video filtering, wireless communications, instrumentation systems and biomedical circuits [111, 112]. Gm-C filters are suitable for biomedical or biological applications because they present high input resistance, it is possible to integrate large time constants within a reasonable silicon area [105] and they have a simple and systematic design flow, but many of their other properties still need improving, such as operation at reduced power consumption [112].

A possible approach to provide low-noise, ultra-low-power, band-pass filtering with amplification, high CMRR and the capacity to reject large input dc values, is to use a traditional Gm-C biquad band-pass filter, for example the one shown in Fig. 4.1 [85, 113]. However, this solution requires an OTA devoted to establish the high-pass characteristic and block the dc input (depicted by Gm3 in Fig. 4.1). This implies an overhead in terms of power consumption and silicon area. There are other Gm-C biquad architectures that achieve the band-pass characteristic without Gm3. However, these architectures, such as the one used in [12], do not have a differential input. These architectures can be used in the middle of the processing chain, but they are not suitable for the input stage. Then, despite to be useful in any context, our solution will be particularly advantageous when a differential input is required.

4.1 Proposed Solution

4.1.1 Input dc block in the traditional biquad

In Fig. 4.1 a traditional biquad implementation of a band-pass filter with amplification is depicted [113]. In order to facilitate the analysis, this discussion will be presented on basis of a particular architecture of a transconductor (symmetrical OTAs). However, the principle is general and can be extended to other OTAs implementations. Then,

Gm1, Gm2, Gm3 and Gmf are symmetrical OTAs whose transconductances are, respectively, G_{m1}, G_{m2} G_{m3} and G_{mf}. We shall refer as $2.IDj$ to the tail current of the input differential pair of Gmj (where j stands for 1, 2, 3 or f).

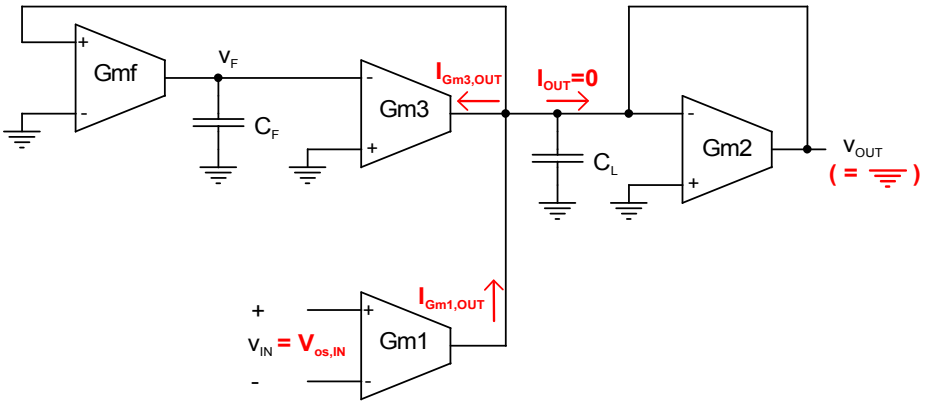


Figure 4.1: Traditional biquad architecture of a band-pass filter with amplification [113] p. 847. The input dc blocking mechanism is highlighted: if $V_{os,IN}$ is a dc signal, v_{OUT} will be zero whenever Gm3 is able to drain the Gm1 ouput current ($I_{Gm1,OUT}$). This means that $I_{Gm3,OUT}$ has to be equal to $I_{Gm1,OUT}$. If Gm3 is not able to provide the needed current, the dc input signal won't be blocked and the band-pass characteristic will be lost.

Gm3 is especially dedicated to establish the high-pass characteristic and block the dc input. Indeed, as shown in Fig. 4.1, any dc input signal $V_{os,IN}$ will generate a current at the Gm1 output ($I_{Gm1,OUT}$), that will be compensated by Gm3, in order to keep the output voltage v_{OUT} equal to zero (at ground voltage). This compensation will be done by means of the integrator Gmf-C_F. For instance, if $I_{Gm1,OUT}$ rises, then v_{OUT} will rise (Gm2 acts as a resistor to ground), then Gmf will increase its output current and v_F will rise as well, hence the Gm3 output current ($I_{Gm3,OUT}$) will fall. The equilibrium will be reached when $I_{Gm1,OUT} = I_{Gm3,OUT}$.

It is worth to emphasize that it is incorrect to analyze the blocking of the dc input solely on basis of the small signal analysis. This would lead to the wrong conclusion that Gm3 is able to block any level of input dc signal. A large-signal analysis shows that the maximum current that Gm3 is able to provide[1] is $I_{Gm3,OUT} = 2.ID3$, when its input differential pair is totally unbalanced, being $2.ID3$ the tail current of the input differential pair of Gm3. Next, if we consider an arbitrary dc input signal $V_{os,IN}$, then $I_{Gm1,OUT} = G_{m1}.V_{os,IN}$. Hence, the maximum dc input signal that this architecture will be able to block is given by Eq. 4.1.

$$V_{os,IN} \leq 2.ID3/G_{m1} \tag{4.1}$$

4.1.2 Description of the proposed architecture

In this chapter we propose a change in a traditional biquad, aiming to reduce the overhead in terms of power consumption and silicon area that Gm3 introduces. We propose to replace Gm3 with the architecture described in Section 3.2.2. This circuit rejects the dc component at the output branch of Gm1 and set the high-pass frequency (see Fig. 4.2). The circuit is formed by the transistors M6, M7, M8 and M9 (see Fig.

[1]For the sake of simplicity, and without loss of generality, we have assumed that the copy factor of the symmetric OTA current mirrors is 1:1.

4.3). Note that in order to maintain the circuit behavior it is necessary to swap the inputs of Gmf.

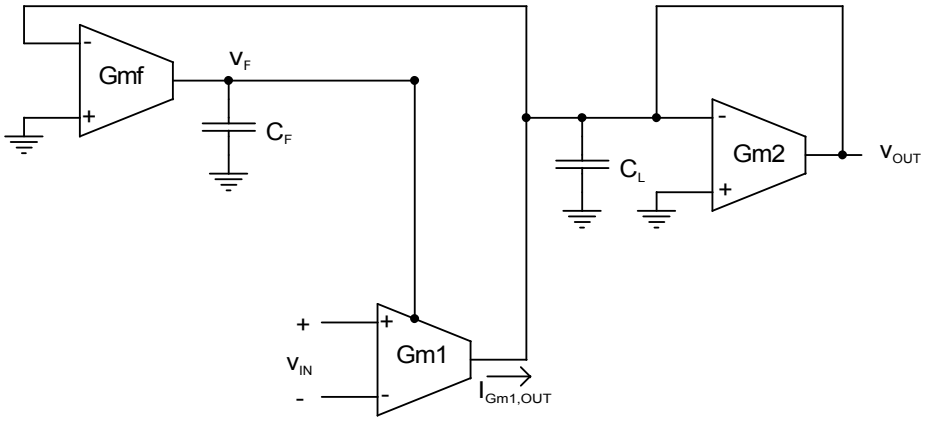


Figure 4.2: Proposed circuit architecture.

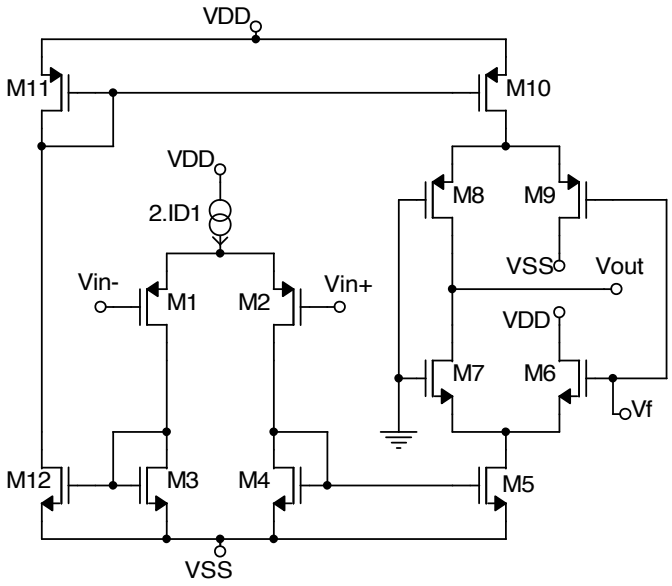


Figure 4.3: Gm1 implementation at transistor level. M6-M9 are part of the dc block circuit.

Gm2 and Gmf are symmetrical OTAs whose respective transconductances are G_{m2} and G_{mf}. Gm1 is an OTA with a differential input (v_{IN}) and a single ended input (v_F). This single ended input is used in a local feedback loop at the output for dc blocking. The transfer function of Gm1 is given by Eq. 4.2 (see Fig. 4.3).

$$i_{Gm1,OUT} \cong G_{m1} v_{IN} + (g_{m6} + g_{m9}) v_F \tag{4.2}$$

where G_{m1} is the Gm1 transconductance and g_{m6} and g_{m9} are the transconductance of M6 and M9; with $gm_7 \gg gm_6$ and $gm_8 \gg gm_9$, where g_{m7} and g_{m8} are the transconductance of M7 and M8.

Following the same reasoning made in Section 3.2 it can be shown that the circuit depicted in Fig. 4.2 has the first-order band-pass transfer function presented in Eq. 4.3.

$$\frac{v_{out}}{v_{in}} = \frac{\frac{G_{m1}}{C_L}s}{s^2 + \frac{G_{m2}}{C_L}s + \frac{(g_{m6}+g_{m9})G_{mf}}{C_L C_F}} \tag{4.3}$$

and the low-pass frequency $f_{low-pass}$ is given by Eq. 4.4, the band-pass gain G by Eq. 4.5 and the high-pass frequency $f_{high-pass}$ by Eq. 4.6.

$$f_{low-pass} = \frac{G_{m2}}{2\pi C_L} \tag{4.4}$$

$$G = \frac{G_{m1}}{G_{m2}} \tag{4.5}$$

$$f_{high-pass} = \frac{(g_{m6} + g_{m9})}{G_{m2}} \frac{G_{mf}}{2\pi C_f} \tag{4.6}$$

The noise performance of both architectures, the traditional biquad (Fig. 4.1) and the proposed architecture (Fig. 4.2), is similar and mainly depends on the design of Gm1 and Gm2 (transistor size and transistor inversion level of the input pairs and the current mirrors). Both architectures can provide excellent results in terms of noise. In addition, as mentioned in Chapter 3, the gain and bandpass cut-off frequencies of these architectures are set by means of parameters that are, respectively, very accurate (i.e. ratios of transconductances) or can be easily and automatically tuned (i.e. ratios of transconductance over capacitances) [85], making it possible to achieve high accuracy without jeopardizing power consumption [86].

In summary, this architecture is suitable for low-noise ultra-low-power operation, presents high CMRR, offers an efficient way to block dc input signals and has a well-controlled high-pass frequency.

4.2 Filter implementation

Biquad filters can be used to address different applications. Therefore, in Table 4.1 we present filter specifications that tries to cover a wide range of applications (audio signals, sensor signals, biological/biomedical signals, etc.) without focusing on any in particular.

Based on the specifications established in Table 4.1, two filters were designed and compared. While the first was based on our novel approach (Fig. 4.2), the second was based on a traditional implementation (Fig. 4.1).

Table 4.1: Filter specifications.

$f_{low-pass}$	7 kHz
$f_{high-pass}$	5 Hz
Gain G	100 V/V
Input dc block	40 mV
CMRR	80 dB

The filters were designed and simulated on a 0.5 μm CMOS technology. The following values were used: $C_L = 2$ pF, $C_F = 300$ pF, $V_{DD} = 1.65$ V and $V_{SS} = -1.65$ V. The value of C_L was set to emulate a typical load capacitance. The value of C_F was

chosen based on the low value of the required high-pass frequency, balancing the trade-off between the large area that implies a large capacitor and the need of implementing an ultra-low-value Gmf transconductor.

4.2.1 Proposed architecture

Given C_L and $f_{low-pass}$, then G_{m2} is set by Eq. 4.4. Hence, as G is given, G_{m1} is set by Eq. 4.5. In order to reduce noise and power consumption, the Gm1 input differential pair is biased in weak inversion (i.e. $(g_m/I_D)_1 \geq 20\ \mathrm{V}^{-1}$), then I_{D1} is set. In order to increase the input linear range of Gm2 (which is equal to the maximum expected output amplitude), the Gm2 input differential pair is biased in strong inversion (i.e. $(g_m/I_D)_2 \leq 5\ \mathrm{V}^{-1}$) and I_{D2} is set.

According to the discussion presented in Section 3.2.2, α was set to 10. Finally, Gmf, g_{m6} and g_{m9} were established by the means of Eq. 4.6 and considering the following trade-off. Initially, it is desirable to have low values of Gmf, g_{m6} and g_{m9}, either to lower the high-pass frequency or to reduce the size of C_F. Secondly, low values of Gmf need very large transistors which imply excessively high C_{gs} values (which affects the low-pass frequency).

Table 4.2 presents the main parameters of the filter transconductors and Table 4.3 the parameters of the dc block circuit.

Table 4.2: Filter main parameters (new approach).

	Gm1	Gm2	Gmf
$(g_m/I_D)_{InDifPar}$	23.3 V^{-1}	5.0 V^{-1}	18.8 V^{-1}
I_D	352 nA	17.4 nA	44 pA
Gm	8.2 μS	87.2 nS	834 pS
$(W/L)_{InDifPar}$ (μm/μm)	38.8/1.2	1.5/152	1.5/1294

Table 4.3: Dc block circuit parameters (new approach).

g_{m6}	387 nS
$(W/L)_{M6}$	1.5/36 (μm/μm)
g_{m7}	3.66 μS
$(W/L)_{M7}$	1.5/36 (μm/μm)
g_{m8}	4.36 μS
$(W/L)_{M8}$	1.5/8.3 (μm/μm)
g_{m9}	411 nS
$(W/L)_{M9}$	1.5/8.3 (μm/μm)

4.2.2 Traditional implementation

The design process is similar to the one carried out in the previous section. The only difference concerns the setting of the high-pass frequency. In this case, Gm3 has to be sized instead of Gmf, g_{m6} and g_{m9}. For this purpose, Eq. 4.1 (which implies that $ID3 > 164$nA) and $f_{high-pass} = \frac{G_{m3}G_{mf}}{2\pi C_F G_{m2}}$ will be the design equations. Table 4.4 shows the main parameters of the resulting design for the traditional biquad architecture.

Table 4.4: Filter main parameters (traditional approach)

	Gm1	Gm2	Gmf	Gm3
$(g_m/I_D)_{InDifPar}$	23.3 V^{-1}	5.0 V^{-1}	18.8 V^{-1}	5.0 V^{-1}
I_D	352 nA	17.6 nA	44 pA	176 nA
Gm	8.2 μS	87.6 nS	834 pS	883 nS
$(W/L)_{InDifPar}$ (μm/μm)	38.8/1.2	1.5/152	1.5/1294	1.5/15.2

4.3 Results

Monte Carlo (MC) mismatch simulations (100 runs), at transistor level, of the ac, dc, noise and transient analysis were performed in both implementations. I_{DD} is the total current consumption of the filter, v_{ni} is the input-referred noise voltage, the "Output Offset" is the dc voltage deviation from the reference at the output, PSRR+ is the positive power supply rejection ratio (V_{DD}) and PSRR- is the negative power supply rejection ratio (V_{SS}). The "Input Linear Range" is determined by the maximum input voltage where the THD of the output voltage remains equal or less than 5%.

4.3.1 Proposed architecture

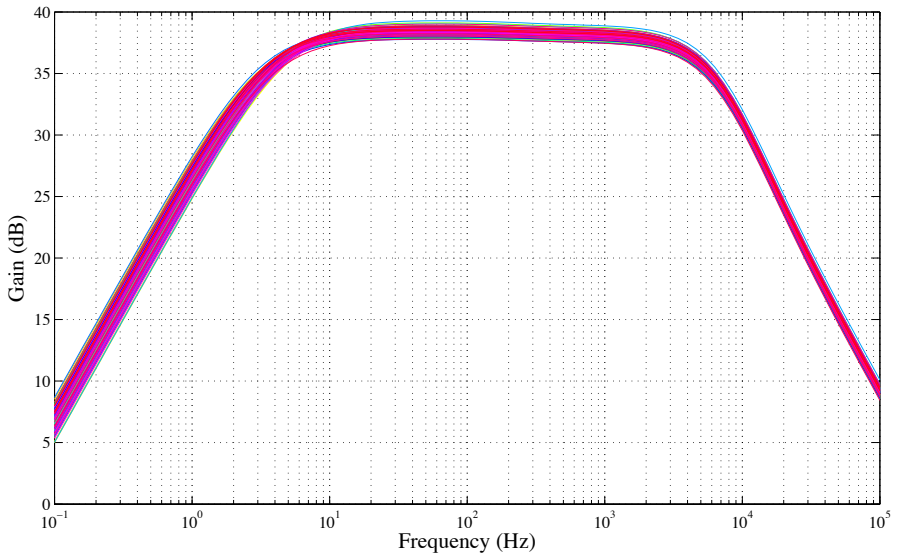


Figure 4.4: MC simulations of the filter frequency response (proposed architecture).

Fig. 4.4 depicts the MC simulations of the filter frequency response of the new approach.

In Table 4.5 the simulated main filter characteristics are presented. The MC simulation mean value of the output dc voltage was 1.3 mV and the standard deviation σ = 4.6 mV. Therefore we have a systematic offset of 1.3 mV and taking $\pm 3\sigma = \pm 13.8$ mV the worst case of the output voltage would be 15.1 mV.

Ac, dc and transient simulations were performed in order to test the blocking of a dc input $V_{os,IN}$. In Table 4.6 the variations of the filter main parameters are

Table 4.5: Filter characteristics (New and Traditional approach).

	New approach		Traditional approach	
	Typical value	Worst case (of 100 runs)	Typical value	Worst case (of 100 runs)
Gain G	38.5 dB	37.8 dB - 39.3 dB	39.54 dB	38.9 dB - 40.2 dB
$f_{low-pass}$	5.4 kHz	5.4 kHz - 5.5 kHz	5.4 kHz	5.3 kHz - 5.9 kHz
$f_{high-pass}$	3.8 Hz	3.1 Hz - 4.6 Hz	4.6 Hz	4.3 Hz - 4.6 Hz
CMRR	89.5 dB	76.6 dB	90.0 dB	76.0 dB
PSRR+	53.5 dB	51.0 dB	58.6 dB	57.7 dB
PSRR-	65.9 dB	61.2 dB	88.5 dB	81.5 dB
Output Offset	1.3 mV	15.1 mV	1.9 mV	16.3 mV
I_{DD}	1.51 μA	-	2.18 μA	-
v_{ni}	14.1 μV_{rms}	-	17.1 μV_{rms}	-
Input Linear Range	8.7 mV_{pp}	-	8.0 mV_{pp}	-

presented. For the transient analysis, the input was a sinusoidal signal of amplitude equal to 100 μV_{pp} and a frequency of 1 kHz.

Table 4.6: Filter response to an input dc offset $V_{os,IN}$ (New and Traditional approach).

	New approach				Traditional approach			
$V_{os,IN}$	Gain G	I_{DD}	THD	$f_{high-pass}$	Gain G	I_{DD}	THD	$f_{high-pass}$
-100 mV	26.8 dB	1.48 μA	0.37%	3.4 Hz	-	-	-	-
-50 mV	35.1 dB	1.48 μA	0.35%	4.6 Hz	-	-	-	-
-45 mV	35.6 dB	1.48 μA	0.35%	4.6 Hz	37.3 dB	2.18 μA	0.37%	1.1 Hz
-10 mV	38.4 dB	1.48 μA	0.35%	3.4 Hz	39.4 dB	2.18 μA	0.37%	4.4 Hz
0 mV	38.5 dB	1.51 μA	0.35%	3.8 Hz	39.5 dB	2.18 μA	0.37%	4.6 Hz
10 mV	38.3 dB	1.56 μA	0.35%	4.3 Hz	39.4 dB	2.18 μA	0.37%	4.5 Hz
45 mV	35.7 dB	1.81 μA	0.35%	5.4 Hz	37.3 dB	2.18 μA	0.37%	1.2 Hz
50 mV	35.1 dB	1.84 μA	0.36%	5.5 Hz	-	-	-	-
100 mV	26.6 dB	2.05 μA	0.37%	4.0 Hz	-	-	-	-

For the input linear range analysis, a 1 kHz sinusoidal signal was taken, and the input was varied from 100 μV_{pp} to 10 mV_{pp}. The results are presented in Table 4.7.

Table 4.7: Filter input linear range (new approach).

v_{IN} (mV_{pp})	v_{OUT} (mV_{pp})	THD (%)
0.1	8.4	0.4
3.5	289	1.0
7.5	670	3.0
8.7	816	4.9
9.0	860	5.6
9.5	940	7.1
10.0	1031	9.0

Table 4.8 presents process corners simulations of gain, high-pass frequency, low-pass frequency and dc blocking capacity. Both mismatch simulations presented in Table 4.5 and process corners simulations presented in Table 4.8 show that the varia-

tions are acceptable.

Table 4.8: Process corner simulation (New approach): worst case speed (wcs), worst case power (wcp), worst case zero (wc0), worst case one (wc1) and typical (typ).

	$V_{os,IN}$ = 0 V			$V_{os,IN}$ = 100 mV		
Corner	Gain G	$f_{low-pass}$	$f_{high-pass}$	Gain G	$f_{low-pass}$	$f_{high-pass}$
wcs	38.7 dB	4.9 kHz	3.7 Hz	27.6 dB	4.9 kHz	4.1 Hz
wcp	38.2 dB	5.9 kHz	3.8 Hz	25.7 dB	5.9 kHz	3.8 Hz
wc0	38.4 dB	5.4 kHz	3.8 Hz	26.4 dB	5.4 kHz	3.8 Hz
wc1	38.5 dB	5.3 kHz	3.8 Hz	27.0 dB	5.3 kHz	3.9 Hz
typ	38.5 dB	5.4 kHz	3.8 Hz	26.6 dB	5.4 kHz	4.0 Hz

In order to confirm the stability of the loop of Gmf and Gm1, an open loop simulation was performed for three values of input dc voltage $V_{os,IN}$ = [-100 mV, 0 V, 100 mV]. The result depicted in Fig. 4.5 shows that the loop has a large phase margin in all conditions. This is related to the dominant pole set by Gmf and C_F, which set the high-pass characteristic of the overall filter.

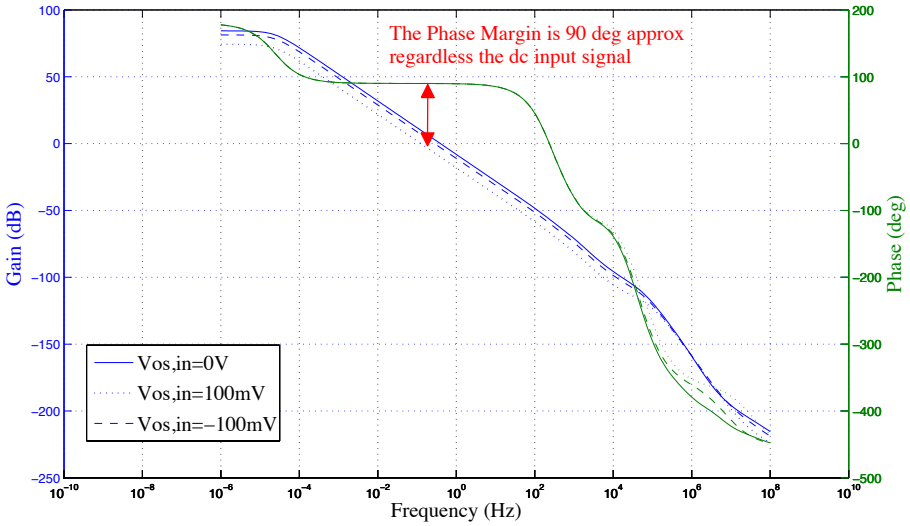


Figure 4.5: Gm1-Gmf Open-loop frequency response (proposed architecture).

4.3.2 Traditional implementation and comparison

In Table 4.5 the main results of the traditional implementation are presented.

Ac, dc and transient simulations were performed in order to test the blocking of a dc input $V_{os,IN}$. In Table 4.6 the variations of the filter main parameters are presented. For the transient analysis, the input was a sinusoidal signal of amplitude equals to 100 μV_{pp} and a frequency of 1 kHz.

From Table 4.5, it can be seen that both filters comply with the specifications established in Table 4.1. The main difference is that the new approach reduced the power-consumption by 30.7%.

The second main difference is that our approach is able to block a dc input of 100 mV (or even higher) while the traditional one lost its high-pass characteristic from a dc input of 50 mV on, as shown in Table 4.6.

An increment of $V_{os,IN}$, reduces the gain G and slightly modifies the high-pass frequency $f_{high-pass}$ in both implementations. In our approach the loss of gain is a bit higher, but it has to be pointed out that our implementation continues to give the band-pass characteristic regardless of the dc input. In order to achieve this behavior with the traditional implementation, its power consumption must be increased.

Finally, it is noted that the PSRR- of the traditional approach is higher than the one presented by the new approach. However, the value achieved by the new approach is acceptable for the considered applications.

Table 4.9 compares differential input second order active band-pass filters reported in the literature. Since these filters were designed for different applications, their main characteristics are different, therefore the comparison has to be done carefully. The usage of capacitors to block dc signals allows to block almost any level of input dc signal but it decreases the value of the CMRR [57,114–116]. On the other hand, filters based on the traditional approach achieve higher CMRR values but are not able to block high levels of input dc signals [86,117,118]. To summarize, Table 4.9 shows that the new approach is an efficient way to balance the trade-off between high precision in setting $f_{high-pass}$, high CMRR and dc input signal blocking capacity.

4.4 Conclusions

In this chapter, we have shown that a significant part of the power consumption of a traditional biquad, is associated with the feedback loop that set the high-pass frequency and blocks the dc input signals. It was also shown that the power consumption of this feedback loop is dictated by the current that this circuit needs to provide in order to compensate the current due to the dc voltage at the input.

Then, we have proposed a modification in a traditional Gm-C biquad filter implementation, using the technique presented in Chapter 3, that efficiently blocks the dc input and set the high-pass frequency.

The proposed architecture presents, as the traditional approach does, a trade-off between gain and dc input blocking capacity. In our approach the loss of gain is greater than in the traditional approach, but it is remarkable that our implementation does not lose the band-pass characteristic for high dc input values. Therefore, it is possible to exchange gain for dc input blocking capacity.

This architecture avoids the overhead in terms of power consumption and silicon area that traditional approaches introduce for establishing the high-pass characteristic and to block the dc input. This feature enables lower power consumption or higher levels of dc input to be blocked without jeopardizing the power consumption. Results from MC simulations show that the proposed architecture, compared with a traditional one, presents a 30% reduction in power consumption and more than doubles the dc input that can be blocked.

Table 4.9: Comparison of the proposed filter with other differential input 2nd order active band-pass filters

	[115]	[116]	[117]	[118]	[86]	[114]	[57]	This work
Bandwidth (Hz) Δf or f_C/Q	1.5-370	2.0k/3	1.95/0.5	2.5k/1	660/1	10k	25m-7.2k	4-5.2k
Gain G	32 dB	0 dB	32.9 dB	0 dB	73 dB	0 dB	39.5 dB	38.5 dB
Power	1 nW	2.85 μW	6.31 μW	16 μW	290 nW	3.36 μW	80 μW	4.98 μW
Input noise v_{ni} (μV_{rms})	27	58	791	38	100	433	2.2	14
CMRR	60 dB @ 100 Hz	N/A	N/A	27 dB @ 1 kHz	N/A	N/A	42 dB worst-case	77 dB worst-case
Dc input amplitude bounded	No	No	Yes	Yes	Yes	No	No	No
Precise $f_{high-pass}$	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes
Dynamic Range (@THD)	50 dB (N/A)	64 dB (1%)	51 dB (1%)	63 dB (1%)	51 dB (2%)	66 dB (5%)	69 dB (1%)	50 dB (5%)
Voltage supply	0.6 V	N/A	3.0 V	1.2 V	1.8 V	2.8 V	5.0 V	3.3 V
Technology	65 nm	0.35 μm	0.35 μm	0.35 μm	0.35 μm	1.5 μm	1.5 μm	0.5 μm
Application	ECG	Audio, Vibration	IR Sensor	Hearing Aids	Biomed. Device	Bionic Ears	Neural Amplifier	Multiple Purpose
Architecture	Alternat. Gm-C	Alternat. Gm-C	Trad. approach	Trad. approach	Trad. approach	Active RC	Active RC w/ pseudo-resist.	New approach

N/A=Not Available

Chapter 5

Integrated programmable analog front-end

In this chapter we introduce the design and simulation of an integrated analog front-end architecture formed by the preamplifier presented in Chapter 3 and two additional band-pass amplifying stages based on the filter architecture presented in Chapter 4. This chapter is an extended version of [31], gathering material from [32] as well as unpublished work.

The goal of this chapter is to present an architecture suitable for acquiring a wide range of low-amplitude physiological signals, such as EEG, visual evoked potentials, LFP, spikes, among others. These signals may come from skin electrodes, cortical arrays or nerve cuffs. As shown in Chapter 2, the amplitude of these signals ranges from 10 μV_{pp} to 1 mV_{pp} (thus require a very low-noise amplification) and its bandwidth ranges from 0.1 Hz to 5 kHz. In addition, the targeted applications require to separate these low level signals from other biological or external interfering signals appearing in common mode, leading to a minimum CMRR requirement that may reach more than 80 dB. Finally, low power consumption suitable for wearable or implantable implementations must be achieved.

5.1 Architecture

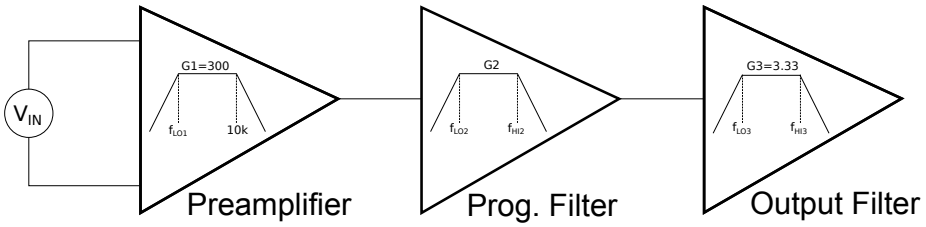


Figure 5.1: Front-end block diagram.

The proposed front-end consists of three stages (see Fig. 5.1). The first stage is implemented using the preamplifier described in Chapter 3. The second stage is a programmable band-pass filter and the third stage is a low-gain high-linear-range band-pass output filter, both stages were designed using the architecture presented in

Chapter 4. Why this is a suitable solution will come up once the main trade-offs of the acquisition chain design are presented in the next subsections.

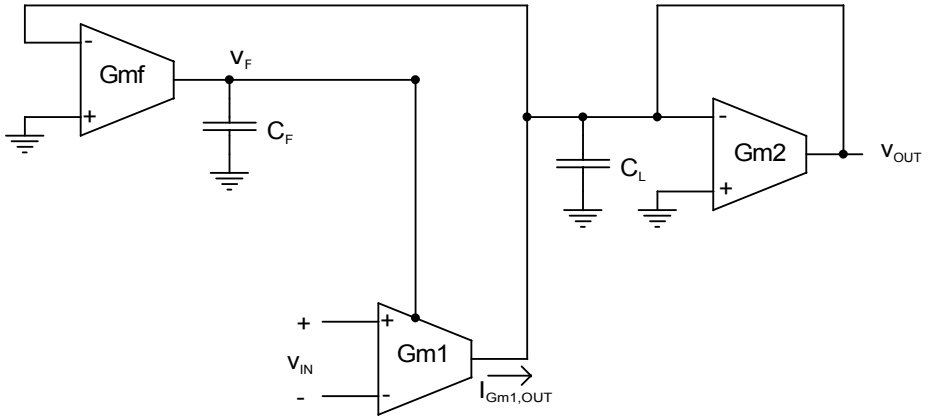


Figure 5.2: schematic diagram of each front-end stage. Gm1 preamplifier is implemented with a single-stage circuit (see Fig. 3.2). Gm1 of the programmable filter and the Gm1 of the output filter are implemented with symmetrical OTAs (see Fig. 4.3). Gm2 and Gmf are symmetrical OTAs on the three cases (see Fig. 3.2).

The schematic diagram of each front-end stage is shown in Fig. 5.2. While the Gm1 preamplifier is implemented with a single-stage circuit (see Fig. 3.2), the Gm1 of the programmable filter and the Gm1 of the output filter are implemented with symmetrical OTAs (see Fig. 4.3). In all cases, Gm1 has a differential input (v_{IN}), a single ended input (v_F) and its transfer function is given by Eq. 5.1:

$$i_{Gm1,OUT} = G_{m1} v_{IN} + g_{mC} v_F \tag{5.1}$$

where g_{mC} is an internal parameter related to the input dc block circuit[1].

Gm2 and Gmf are symmetrical OTAs on the three cases (see Fig. 3.2). A detailed description of the architecture can be found in Chapters 3 and 4. As shown on these chapters each front-end stage has a band-pass transfer function given by Eq. 5.2, where the low-pass frequency $f_{low-pass}$ is given by Eq. 5.3, the band-pass gain G by Eq. 5.4 and the high-pass frequency $f_{high-pass}$ by Eq. 5.5.

$$\frac{v_{out}}{v_{in}} = \frac{\frac{G_{m1}}{C_L} s}{s^2 + \frac{G_{m2}}{C_L} s + \frac{g_{mC} G_{mf}}{C_L C_F}} \tag{5.2}$$

$$f_{low-pass} = \frac{G_{m2}}{2\pi C_L} \tag{5.3}$$

$$G = \frac{G_{m1}}{G_{m2}} \tag{5.4}$$

$$f_{high-pass} = \frac{g_{mC}}{G_{m2}} \frac{G_{mf}}{2\pi C_F} \tag{5.5}$$

In the following subsections we discuss the main trade-offs that this architecture, the application's requirements and the process technology present. Next, in Section 5.2 we present how they were addressed.

[1] In the case of the preamplifier $g_{mC} = g_{m5} + g_{m6}$, where g_{m5} and g_{m6} are the transconductance of M5 and M6 (see Fig. 3.2). In the case of the other two stages, $g_{mC} = g_{m6} + g_{m9}$, where g_{m6} and g_{m9} are the transconductance of M6 and M9 (see Fig. 4.3).

5.1.1 Noise gain trade-off

If the preamplifier input-referred noise voltage is v_{ni1}, then its output-referred noise voltage is $v_{no1} = G_1 v_{ni1}$, where G_1 is the preamplifier gain (in general we will note G_i as the gain of the ith stage). If the input-referred noise voltage of the second stage is v_{ni2}, and we impose that the noise contribution of the second stage adds only a 10% to the noise given by the first stage in the total input-referred noise voltage v_{ni2}^{total}, then we have:

$$v_{ni2}^{total} = \sqrt{v_{no1}^2 + v_{ni2}^2} < 1,1 v_{no1} \tag{5.6}$$

Thus,

$$v_{ni2} < 0,46 . G_1 v_{ni1} \Rightarrow G_1 > 2,18 . \frac{v_{ni2}}{v_{ni1}} \tag{5.7}$$

Eq. 5.7 is a very useful design equation that shows how the noise requirement define the preamplifier gain. The preamplifier is one of the main contributors to consumption due to its low noise requirement (Eq. 2.3). To reduce consumption, we should enable the second stage to have higher noise, which lead to the need of a high gain in the first stage. For instance, if we impose that $v_{ni1} = 2\ \mu V_{rms}$ and $v_{ni2} = 250\ \mu V_{rms}$, we will have:

$$G_1 > 2,18 . \frac{v_{ni2}}{v_{ni1}} = 2,18 . \frac{250}{2} \Rightarrow G_1 > 273 V/V \tag{5.8}$$

5.1.2 Linearity gain trade-off

Our architecture uses transconductors instead of operational amplifiers. This approach is very advantageous in terms of power consumption but faces linearity problems. A transconductor with a standard input differential pair is not able to efficiently handle an input signal much higher than 300 mV_{pp} (see [104]). Therefore, if the input signal ranges from 10 μV_{pp} to 1 mV_{pp}, the preamplifier gain G_1 should be:

$$G_1 \leq 300 V/V \tag{5.9}$$

This ensure that the signal amplitude at the preamplifier output, and therefore at the inputs of Gm2 and Gmf (see Fig. 5.2), be less or equal than 300 mV_{pp}.

The same restriction applies to the second stage. If $G_1 = 300$ V/V, the signals at the programmable filter input ranges from 3 mV_{pp} to 300 mV_{pp}. In order to assure that the signal amplitude remains below 300 mV_{pp}, the programmable gain G_2 have to vary between 1 V/V (for the signals in the 300 mV_{pp} range) and 100 V/V (for the 3 mV_{pp} signals).

If the third stage has to provide additional amplification, some change in the architecture will be necessary.

5.1.3 Linearity noise current-consumption trade-off

As introduced Section 3.2.5 and graphically shown in Fig 3.5, the design of the OTAs of this architecture, but particularly Gm2, present a trade-off between current consumption, noise and linearity. The inversion level of the input differential pair of Gm2 (related to $(g_m/I_D)_2$) is a useful tool to evaluate this trade-off. A low value of $(g_m/I_D)_2$ (strong inversion) implies a higher input linear range but also more current consumption and more noise. On the other hand, a high value of $(g_m/I_D)_2$ (weak inversion) set a narrower input linear range while current consumption and noise are reduced. Depending on the application, moderate inversion could be a good choice.

5.1.4 Transconductance value and programmability constraints

It can be seen from Eqs. 5.3, 5.4 and 5.5 that in order to program the gain we need to vary the transconductance values, and possibly also the capacitor values, to program the cut-off frequencies. In order to modify the transconductance value we may vary the bias current of the transconductor or we may modify the internal structure of the transconductor (e.g. the current mirror gain factor).

According to Eq. 5.3, given $C_L = 2$pF, in order to vary $f_{low-pass}$ between 100 Hz and 5 kHz, $Gm2$ has to vary between 1.3 nS and 63 nS. Thus, $Gm2$ has to vary by a factor of 50. This cannot be done by just modifying the Gm2 bias current because the Gm2 input differential needs to be biased in strong inversion to provide the required linearity and if we change the bias current by a factor of 50 either the differential pair will no longer be in strong inversion or the dc voltages (V_{GS}, V_{DSsat}) will vary too much. In the meantime, if G_2 has to vary between 1 V/V and 100 V/V, according to Eq. 5.4, $Gm1$ must vary between 1.3 nS and 6.3 μS. This means that $Gm1$ has to vary by a factor of 5000. This situation can be relaxed by tuning C_L. Achieving these large factors is an interesting challenge, in Section 5.2 we present how it was addressed.

5.1.5 Dc-block gain trade-off

As discussed in Chapter 3, our architecture offers a trade-off between gain and dc-block capacity. This trade-off is ruled by the parameter α introduced in Section 3.2.2. A low value of α enables higher levels of dc-block capacity jeopardizing gain. On the other hand, a high value of α reduces the dc-block capacity while gain remains unaffected.

5.1.6 Capacitor size constraints

According to Eq. 5.5, in order to achieve sub-1Hz high-pass frequencies it is necessary to work with sub-nS OTA (which is perfectly feasible, see [105]) and/or use relatively large capacitors ($200 - 300$ pF).

5.2 Implementation

The balance between the constraints and trade-offs presented in the previous section led to the following design decisions. The programming is performed in the intermediate stage, where it is not necessary to filter very small signal amplitudes (and thus the noise is no longer a major problem) nor very large signal amplitudes (where the linearity starts to be a problem). The preamplifier has a $G_1 = 50$ dB fixed gain. The gain of the second stage (G_2) can be programmed between 0 dB and 40 dB and the low-pass frequency between 100 Hz and 5 kHz. The output filter has a $G_3 = 10$ dB fixed gain, so its linear range at the output should be 1 V_{pp}. In order to achieve this linear range, the linearization technique employing source degeneration proposed by [119] was implemented in the output stage.

In order to program the gain and the low-pass frequency of the second stage we designed a *Base Filter* with the maximum gain ($G = 40$ dB) and the maximum desired low-pass frequency ($f_{low-pass} = 5$ kHz). The first and third stage were designed to have a cut-off frequency higher than $f_{low-pass} = 5$ kHz in order to warrant that the whole front-end can reach a $f_{low-pass} = 5$ kHz.

We implemented two mechanisms to program the gain of the Base Filter. First, a *rough tuning* was implemented by modifying the copy factor at the output current mirror of Gm1 (this allows to divide $Gm1$ by 10 or 100). Second, a *fine tuning* was achieved by varying the Gm1 Bias current (this permits to divide $Gm1$ continuously by

up to 8 times). The low-pass frequency was programmed varying the value of C_L. This was done by connecting in parallel (by means of switches) various integrated capacitors of different values in order to obtain six discrete values of C_L (C_L = [1.6 pF, 3.3 pF, 10 pF, 20 pF, 33.3 pF, 100 pF] which respectively set $f_{low-pass}$ = [5 kHz, 3 kHz, 1 kHz, 500 Hz,300 Hz, 100 Hz]).

The input dc value that the programmable filter and the output stage have to block, corresponds to the output offset of the previous stage, which is not that high (less than 25 mV). Then, for these stages we took $\alpha = 10$, which is a reasonable compromise, because the loss of gain is negligible and the circuit presents an adequate capacity of blocking dc input signals. In the case of the preamplifier, as mentioned in Section 3.3, we took $\alpha = 100$.

For the maximum low-pass frequency setting ($f_{low-pass}$ = 5 kHz) the flicker noise effect is negligible compared to the contribution of thermal noise (this was already mentioned when reporting the preamplifier implementation, see Section 3.3). However, for the minimum $f_{low-pass}$ setting (100 Hz), the effect of the flicker noise is significant. The wide transistors used in the preamplifier are crucial to keep this noise bounded.

Table 5.1 presents the main parameters of the front-end transconductors.

Table 5.1: Front-end main parameters

	Preamplifier	Base Filter (Prog.)	Output filter
G_{m1}	100 μS	6.3 μS	523 nS
G_{m2}	320 nS	63 nS	157 nS
G_{mf}	1.2 nS	1.9 nS	5.7 nS
g_{mC}	360 nS	158 nS	53 nS
C_L	5 pF	2 pF	2 pF
C_F	47 pF	300 pF	300 pF
α	100	10	10

5.3 Results

Monte Carlo (MC) mismatch simulations (500 runs) of the frequency response were performed on the four corners that arise from programming the gain and the low-pass frequency.

Fig. 5.3 depicts the transistor level MC simulations of the front-end frequency response for maximum G and minimum $f_{low-pass}$.

Fig. 5.4 depicts the transistor level MC simulations of the front-end frequency response for maximum G and maximum $f_{low-pass}$.

Table 5.2 presents simulations results for the aforementioned four corners. This table shows that the front-end gain is programmable between 57 dB and 99 dB, the low-pass frequency is programmable between 116 Hz and 5.2 kHz. The maximum power consumption of the front-end is 11.2 μA and its maximum equivalent input-referred noise voltage is 1.87 μV_{rms}. The front-end configured for the maximum gain (99dB) and the maximum low-pass frequency (5.2 kHz), has a consumption of 11.2 μA and its equivalent input-referred noise voltage is 1.46 μV_{rms}, which corresponds to a NEF = 2.61. On the other hand, we note some degradation in terms of current-efficiency (NEF = 14) in the minimum gain and minimum $f_{low-pass}$ setting. However, the performance of this corner, in other parameters of the front-end, is very good. This degradation occurs because we designed a filter (Base Filter) for a higher bandwidth and higher gain, and our programming method (to switch capacitors) is not able to

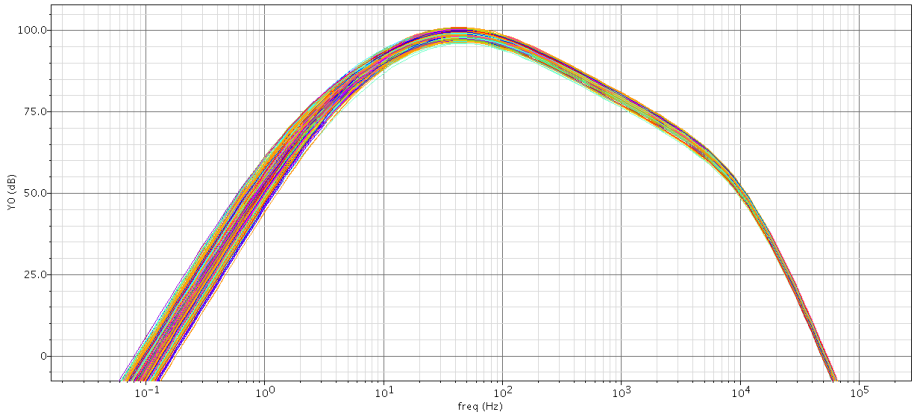


Figure 5.3: Monte Carlo simulations (500 runs) of the front-end frequency response for maximum G and minimum $f_{low-pass}$.

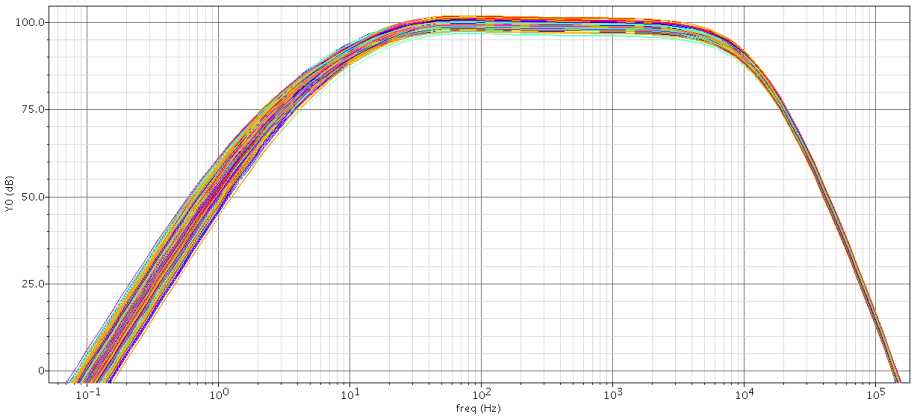


Figure 5.4: Monte Carlo simulations (500 runs) of the front-end frequency response for maximum G and maximum $f_{low-pass}$.

recover in terms of power consumption or noise, the reduction of bandwidth. One possible way to overcome this issue is to explore the possibility of programming the front-end by modifying the Gm1 preamplifier bias current.

The front-end presents a good linearity achieving an output swing of 483 mV_{pp} with a THD = 1.0% and 950 mV_{pp} with a THD = 4.8%.

The performance achieved by relevant prior works that implement complete front-ends [3, 44–47, 62], which reach high gain (greater than 65 dB) and cover the desired bandwidth, are compared with our work (with maximum $f_{low-pass}$ setting) in Table 5.3. The data show that our front-end presents the best results in terms of CMRR and noise, has the greater value of gain, equaling the best NEF reported.

5.4 Conclusions

The most important contribution of this chapter is to have applied a novel architecture to the design of a complete programmable front-end.

Table 5.2: Front-end simulations results.

		Minimum $f_{low-pass}$		Maximum $f_{low-pass}$	
		Mean	σ or Min-Max	Mean	σ or Min-Max
Max Gain	Gain G (dB)	98.9	$\sigma = 0.8$	99.3	$\sigma = 0.8$
	Input noise v_{ni} (μV_{rms})	0.40	$\sigma = 0.03$	1.46	$\sigma = 0.12$
	$f_{low-pass}$ (Hz)	116	115 - 117	5.2k	5.0 k - 5.4 k
	$f_{high-pass}$ (Hz)	17.3	16.9 - 17.8	19.0	18.6 - 20.5
	Supply current (μA)	11.2	-	11.2	-
	NEF	5.19	-	2.61	-
Min Gain	Gain G (dB)	57.3	$\sigma = 1.1$	58.1	$\sigma = 1.1$
	Input noise v_{ni} (μV_{rms})	1.14	$\sigma = 0.03$	1.87	$\sigma = 0.14$
	$f_{low-pass}$ (Hz)	116	121 - 125	4.9k	4.8 k - 5.0 k
	$f_{high-pass}$ (Hz)	17.0	15.8 - 18.1	20.0	19.4 - 20.6
	Supply current (μA)	10.8	-	10.8	-
	NEF	14.5	-	3.39	-

Table 5.3: State-of-the-art front-ends comparison.

	[3]	[62]	[44]	[45]	[46]	[47]	This work
Technology (μm)	Discrete	0.13	0.5	0.18	0.25	0.13	0.5
Max. Gain (dB)	93.4	77.6	78.0	66.0	79.8	65.5	99.3
Min. Gain (dB)	69.4	42.8	67.8	49.0	52.4	47.5	58.1
$f_{low-pass}$ (kHz)	6.5	10.0	8.0	11.7	8.9	6.9	5.2
$f_{high-pass}$ (Hz)	445	300	10	350	4	167	19
Supply current (μA)	3170	75	25	11.1	3.67	1.9	11.2
Input noise (μV_{rms})	1.0	1.95	4.32	5.4	6.67	3.8	1.46
NEF	27.9	6.60	9.30	6.53	5.22	2.46	2.61
$CMRR_{worst\text{-}case}$ (dB)	39	N/A	N/A	N/A	N/A	N/A	82
$CMRR_{measured}$ (dB)	42	63	N/A	66	62	83	87
Prog. $f_{low-pass}$ (kHz)	No	No	No	No	1 - 17	4.8 - 9.8	0.1 - 5.2
Prog. $f_{high-pass}$ (Hz)	No	No	0.1 - 1 k	No	0.1 - 1.2 k	12 - 16	No
THD 1% (mV_{pp})	N/A	1.0	N/A	N/A	N/A	3.1	0.6

N/A=Not Available

The main design trade-offs of the front-end architecture were discussed and their impacts in the design of the acquisition chain in terms of assignment of gain, noise, linearity and programmability to each stage were shown.

Noise is the most critical requirement of the first stage because ultra-low-amplitude signals must be amplified and filtered. Therefore, the noise-power trade-off, expressed in terms of the NEF, led us to assign most of the power budget to the first stage. Furthermore, the noise-gain trade-off and linearity-gain trade-off determined the gains of the first and second stage. Moreover, it was shown that programming wide ranges of gain and/or cut-off frequencies implies wide ranges of transconductance values and high capacitor values.

The integrated programmable analog front-end architecture presented is focused in acquiring a wide range of physiological signals. This can be done because the gain is programmable between 57 dB and 99 dB, and the low-pass frequency is programmable between 116 Hz and 5.2 kHz, while the maximum power consumption of the front-end

is 11.2 μA and its maximum equivalent input-referred noise voltage is 1.87 μV_{rms}.

The comparison between our front-end and other works in the state-of-the-art shows that our front-end presents the best results in terms of CMRR and noise, has the greatest value of gain and equals the best NEF reported.

Chapter 6

A system level perspective

On our way to designing a wireless biopotential recording system based on the architecture proposed in Chapters 3, 4 and 5, we developed three prototypes[1] based on off-the-shelf components [33, 34, 36]. As shown in Chapter 2, the design of these systems faces several challenges. In the first three sections of this chapter we describe these experiences showing how these challenges were addressed. In the final section we conclude with a comparison between the developed systems and other systems in the state-of-the-art.

6.1 Wireless neural recording system

This Section summarizes the work reported in [33], which is a low-power 4-channel wireless neural recording system based on off-the-shelf components, aiming at 12-bits 10 ksps acquisition and real time transmission.

6.1.1 Proposed Solution

The developed system is depicted in Fig. 6.1, a *remote module* is kept by the test subject and a *base module* is connected to a PC. The remote module is composed by a programmable AFE and a system-on-chip (SoC) that implements the digitalization of up to four signals and the communication with the base module. The base module consists of a SoC equal to the one in the remote module. The Graphic User Interface (GUI) was developed as a toolbox in Matlab and besides storing the data in the PC, offers a friendly interface for the user to operate the remote module and visualize and analyze the acquired data.

Analog front-end

In Fig. 6.2 a block diagram of one channel of the AFE is presented. This AFE features a programmable gain between 68 dB and 97 dB, the high-pass frequency is fixed in 0.1 Hz and the low-pass frequency can be set between 200 Hz and 15 kHz. in addition,

[1] These works have been done in the framework of two undergraduate thesis and three research projects. I was the advisor of the two undergraduate thesis, responsible researcher for two projects and member of the third research project. In the three roles, I was fully involved in the design and implementation of the prototypes. I have participated in the system design main decisions, in the definition of the hardware and embedded software architecture, in the planning and execution of tests, and in the results analysis.

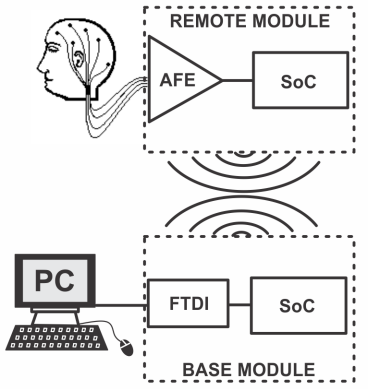


Figure 6.1: High-level description of the neural recording system.

the input-referred noise is less than 11 nV/$\sqrt{Hz}$ (for frequencies greater than 10 Hz), and the measured CMRR is greater than 93 dB.

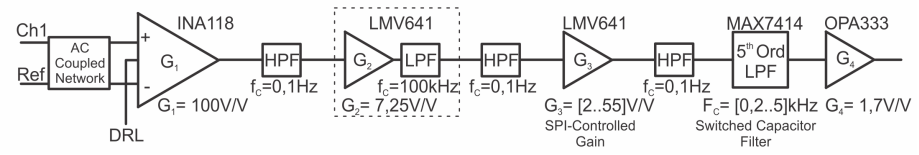


Figure 6.2: Block description of a signal's path through one channel of the AFE.

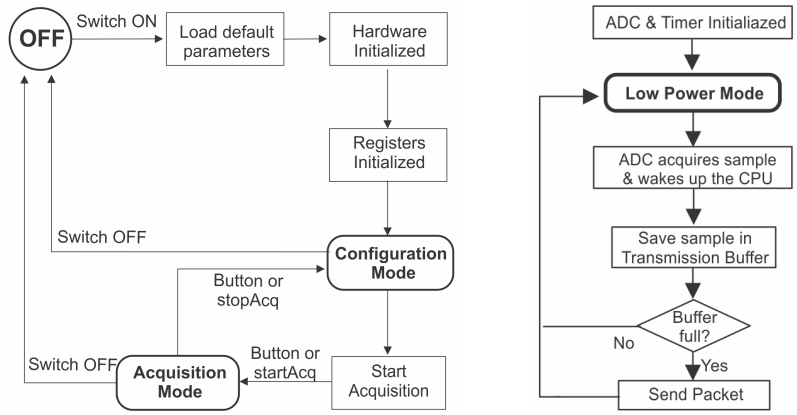
Processing and communication block (SoC)

The signal digitalization and the communication between modules are implemented with a CC430F6137 chip from Texas Instruments (TI). This SoC includes a MSP430 microcontroller (MCU), a CC1101-based sub-1 GHz radio-frequency transceiver, 12-bits ADCs, Timers, and UART (Universal asynchronous receiver-transmitter) and SPI (Serial Peripheral Interface) peripherals. The MCU is a 16-bit RISC microcontroller with a maximum clock frequency of 20 MHz, with 32 kB of Flash and 4 kB of RAM memory. This chip features a typical power consumption of 3.2 mA in *active mode* (at 20 MHz clock frequency and 3.3 V supply voltage) and offers several modes of low-power operation, called *sleep mode*, where its power consumption can be as low as a few of microamperes.

The remote and base module's firmware operates in two modes: *configuration mode* and *acquisition mode*. The main functions of the remote module embedded software are: receive data from AFE, and digitize and send this data to the base module. In addition, is responsible for parsing commands received from the base module. The MCU acts as master in the SPI communication digital potentiometer that controls the gain (AD5270), as well as, to the clock pin of the programmable filter (MAX7414). In Fig. 6.3 the main components of the remote module firmware flowchart are shown. With respect to the base module, in the acquisition mode it works always forwarding packages from the remote module to the PC.

In both modules a round-robin with interrupts architecture is adopted, where interrupt service routines (ISR) are extensively used to exchange (transmit and receive)

data, and keep the MCU in sleep mode while no processing is needed. The ISR in turn use flags to signal in the main loop whether extra processing is needed. If no further processing is needed, the MCU is put in sleep mode.



(a) High level. (b) acquisition mode.

Figure 6.3: remote module firmware flowchart.

For the communication between modules, a packetized system was selected employing 60 bytes for data, 1 byte as counter for detection of lost packets, and 10 bytes internally added by the radio core (8 for synchronization and preamble bytes and 2 for CRC). Each sample is dispatched in 2 bytes, so each packet carries up to 30 samples. The 60 bytes are used during the acquisition mode for sending sampled data, and also during the configuration mode to send programming parameters and consult current configuration. The communication is done over a 915 MHz link with a programmed data rate of 358 kbps. At reception in the base module, the packages are forwarded to the PC through the UART interface, at 921.6 kbps and converted by a FTDI chip into USB protocol.

The sampling frequency, which is configured from the GUI before starting the experiment, may vary between 12 ksps at full speed sampling to 2 ksps in a *battery save mode*.

The acquisition can be started directly from the PC or the system can be commanded to wait until a button, in the remote module, is pressed. Once the acquisition starts, the communication between modules becomes unidirectional from the remote module to the base module, in order to take advantage of all the airtime to transmit the sampled data. To force a stop in the acquisition, the button in the remote module has to be pressed again. Also a time limit can be selected for the test and once reached the system automatically stops.

6.1.2 System test

Power consumption

The average supply current when acquiring 4 channels at 2.5 ksps/ch is 31.2 mA. In this scenario, the system continuously operates for more than 28 hours with two AAA rechargeable batteries (900 mAh). In the battery save mode (4 channels at 0.5 ksps/ch) the average supply current is 7.9 mA and the autonomy is more than 113 hours.

Analog front end

The AFE provided the expected performance, specially with regard to the programmable gain and bandwidth. However, because of the transmission power chosen for the communication, and the fact that the AFE was located close to the antenna, given the modules reduced size, a severe interference in the acquired signals was observed while acquiring with the system from end to end. This was produced by a bad electromagnetic isolation of the AFE. At the time, this problem was mitigated but not fully solved, being one of the milestones for future developments for this work.

Communications

Several scenarios were tested measuring an average of 10 runs for each scenario. In Table 6.1 these averages are reported along with the proposed scenario. These numbers indicates than in most cases the packet-loss rate is around 1%; however, it deteriorates whenever there is obstacle very close to one of the stations. 12 ksps of effective data rate, with a 358 kbps raw data rate, was achieved with a packet loss less than 2% at 5 m distance with a transmit power of 10 dBm. Raw data rates of 407 kbps were tested and can be used at the cost of a higher packet-loss ratio.

Table 6.1: Packet-loss ratio for different scenarios of acquisition

Modules Distance	Obstacle in the line of sight	Packet-Loss Ratio
H: 1.5m; V: 0m	No	0,94%
H: 3.0m; V: 0m	No	1,19%
H: 3.0m; V: 0m	Person	1,26%
H: 4.0m; V: 1.5m	No	1,45%
H: 6.0m; V: 0m	No	1,29%
H: 6.0m; V: 0m	Person	1,68%
H: 6.0m; V: 1.0m	Thick wall of bricks	1,11%
H: 7.0m; V: 0m	No	1,09%
H: 7.0m; V: 0m	Person	1,13%
H: 7.0m; V: 0m	Person close to the base module (0,20m)	3,00%

H = Horizontal, V = Vertical

The effective sampling and transmission ratio depends on the processing load of the SoC. While sampling up to 3 channels and transmitting them at 358 kbps radio data rate, operation at a overall sampling rate of 12 ksps is reached (1 channel at 12 ksps/ch, 2 channels at 6 ksps/ch each or 3 channels at 4 ksps/ch each). Acquisition and transmission of 4 channels requires slowing down the sampling rate to 10 ksps (2.5 ksps/ch per channel).

Full-system test

Signals of different frequency and amplitude were injected directly into the ADC and transmitted. Then the recovered signals were analyzed in the PC, and the Fast Fourier Transform (FFT) was run to recover the principal frequency component. These results show that the received signal is a very accurate approximation of the injected signal. In the Fig. 6.4-A, there is an example of the recovered signal and its FFT in Fig. 6.4-B.

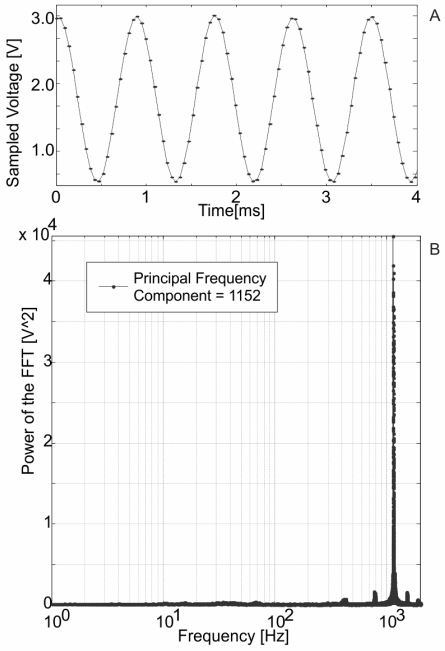


Figure 6.4: Signal acquired by the proposed system (injected directly into the ADC). A) Temporal evolution, B) Fast Fourier Transform (FFT).

6.1.3 Conclusions

A neural signal recording system based on a MSP430 SoC from TI was implemented. The system is capable of acquiring 4 channels at 2.5 ksps/ch encoded in 12 bits and transmit them wirelessly. In this scenario, the average supply current is 31.2 mA, which allow to continuously operates for more than 28 hours with two AAA rechargeable batteries (900 mAh). In the battery save mode (4 channels at 0.5 ksps/ch) the average supply current is 7.9 mA and the autonomy is more than 113 hours. The wireless communication achieved a remarkable throughput of 358 kbps with a packet loss of less than 2 % at 10 dBm transmit power and 5 m distance.

Future developments for the hardware should focus in the integration of the remote module in a single board, substituting the antenna with a PCB antenna and the improvement of the shielding of the AFE against electromagnetic interference.

6.2 Wireless EEG recording system I: WiFi

EEG is one of the main tools used for studying human brain activity. However, current standard EEG systems are wired and uncomfortable, and are mainly used in static settings in clinical practice. As discussed in Chapter 2, in order to enable EEG recordings in daily-life activities, EEG technology needs to become wearable (wireless, low weight, and small size), which requires low-power operation and energy-efficient wireless data transmission. Although a bandwidth ranging from 0.5 Hz to 60 Hz is sufficient for many EEG applications, much higher frequencies (up to 500 Hz) are required in other cases [10]. In addition, the current miniaturization of analog front-ends (AFE) for acquiring EEG signals enables the simultaneous recording of hundreds

of channels [48, 68]. As a consequence, handling high data rates efficiently is essential for high-performance EEG recorders.

A WiFi 64-channel EEG recording system for wearable applications is presented. The aim of this work is to allow the patient to move freely for a reasonable time (about one day) within a short distance (about ten meters), in order to extend the field of application of traditional EEG. In this Section we summarize the work reported in [34].

6.2.1 Proposed solution

The proposed solution, depicted in Fig. 6.5, consists of a wireless module located in the patient and a GUI that runs on a PC.

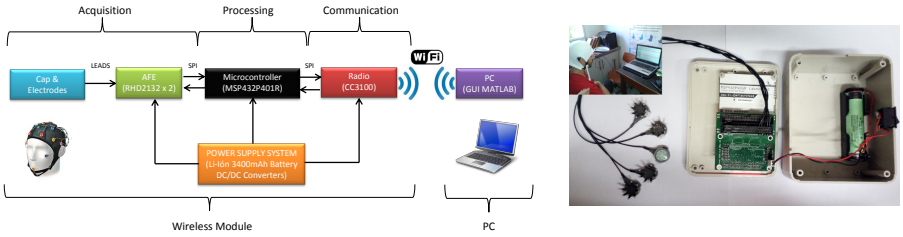


Figure 6.5: WiFi wireless EEG recording system.

At the beginning of the test the user selects the desired system configuration, which implies setting the high-pass ($f_{high-pass}$) and low-pass ($f_{low-pass}$) frequency, the sampling frequency (f_S), the number of channels to be sampled (N_C, that can be selected from four predefined standard electrode arrangement: 1, 4, 21 or 64 channels) and the number of synchronism channels (N_S, up to 6). The synchronism channels allow to record the reaction to a stimulus synchronized with the EEG signals (for example the pressing of a button in front of a visual stimulus to analyze the reaction time). Next, the user gives the command to start in the GUI and the EEG test begins. The data acquisition block samples $N_C + N_S$ channels every $T_S = 1/f_S$ and sends them (via a Serial Peripheral Interface, SPI) to the data processing block, which in turn processes the data and sends them (via SPI) to the data communication block. Finally, this block sends the acquired data (via WiFi) to the PC, where the user can view them in real time.

Data acquisition block

The data acquisition block comprises electrodes, a cap, a programmable AFE, and an ADC. Dry electrodes from Cognionics were used: Flex Sensor to acquire through hair and Drypad Sensor to acquire in skin. The AFE and ADC were implemented using two off-the-shelf RHD2132 chips from Intan Technologies. Each RHD2132 chip is in charge of acquire, amplify, digitize and transmit by SPI (16 bits) up to 32 channels at 30 ksps each. The RHD2132 chip features an input impedance of 1.3 GΩ, a CMRR of 82 dB, low input referred noise (2.4 μV_{rms}), programmable bandwidth and low power operation. For instance, the high-pass frequency can be set between 0.1 Hz and 500 Hz and the low-pass frequency can vary from 100 Hz to 20 kHz. In addition, the total current consumption of the two chips to acquire 64 channels at 500 sps/ch is 1.8 mA and at 1 ksps/ch it is 2.1 mA. A four-layer PCB supporting the RHD2132 chips was carefully designed and fabricated. The top and bottom layers of this PCB were used for signal routing. The second layer was a ground plane and the third layer was a V_{DD} plane.

Data processing block

The data processing block is based on the MSP432P401R microcontroller from TI. This MCU is a 32-bit ARM Cortex-M4F microcontroller with a maximum clock frequency of 48 MHz, with 256 kB of Flash and 64 kB of RAM memory. This chip features a typical power consumption of 4.6 mA in active mode (at 48 MHz clock frequency and 3.3 V supply voltage) and hundreds of nanoamperes in sleep mode. In addition, this MCU includes a rich set of peripherals including several 8-bit SPI ports, UART ports and timers.

The main functions of the MCU embedded software are: receive the sampled data from the RHD2132 chips, process this data and forward them to the WiFi radio module. In addition, the MCU is responsible for parsing commands received from the PC.

A round-robin with interrupts architecture is adopted, where ISRs are extensively used to exchange (transmit and receive) data, and keep the MCU in sleep mode while no processing is needed. The ISR in turn use flags to signal in the main loop whether extra processing is needed. If no further processing is needed, the MCU is put in sleep mode.

The MCU acts as master in the SPI communications. A software 16-bit SPI implementation was developed for the MCU - RHD2132 chips communication. Two different SPI ports of the MCU are used to communicate with the RHD2132 chips. Firstly, to parallelize the data flow, and also to configure the two chips separately. An additional SPI port is used to communicate the MCU with the WiFi radio module.

Two MCU timers are used. One is employed to set the sampling frequency f_S. When this timer expire, the MCU triggers a new acquisition by strobing commands to the RHD2132 chips according to the system configuration and stores the received data into an input buffer. The second timer is used to periodically poll the WiFi radio module input buffer to check for incoming commands from the PC.

Data communication block

The data communication block is implemented with a WiFi radio module based on the CC3100 chip from TI. The WiFi radio module sends the acquired data to the PC, receive commands from the PC as well as exchange configuration parameters. The SimpleLink library provided by the vendor is used to communicate with the WiFi radio module.

The communication technology was selected considering the system requirements, specially maximum data rate, power consumption and communication range to ensure connectivity within the required area. The maximum effective throughput required by the application correspond to acquiring all channels ($N_C = 64$, $N_S = 6$) at the highest data sample rate ($f_S = 1$ kHz) and with the maximum resolution (16 bits per sample), resulting in 1120 kbps. WiFi was chosen, which despite of being a technology with relative high power consumption, it meets the application requirements and gives the chance to scale. In addition, WiFi is widely adopted enabling an almost straightforward integration. The application was build over TCP (Transmission Control Protocol) since it provides a reliable data stream.

6.2.2 System test

Communication

The system requirements imposes a minimum throughput for the payload data of 1120 kbps (see Section 6.2.1). The maximum measured data throughput, at 12 meters

of distance between the wireless module and the router, was 5480 kbps. Although the data throughput was not measured for distances greater than 12 meters, the system has the potential to operate in a greater range.

Acquisition timing

In order to start an acquisition the MCU must establish a communication with both RDH2132 chips, which we will call AFE0 and AFE1. Two possible configurations were analyzed: request all channels to AFE0 first, and then all channels to AFE1 (serial configuration); or, request all channels in parallel to both chips (parallel configuration).

The measured acquisition time[2] for 64 channels ($N_C = 64$ and $N_S = 0$) in the serial configuration was 1.03 ms, and in the parallel configuration was 1.05 ms. Although at first glance it is expected that the parallel configuration would be faster, since there is only one processor, it can not process both interruptions at the same time, and it processes first the interruption of the AFE0 because it has higher priority. Due to the similarity between the serial and parallel configuration delays, it is decided to use the serial one, since it allows a simpler implementation of the embedded software.

Maximum sampling frequency vs. number of channels

The maximum frequency f_S for which the system works without data losses for different system configurations was measured carrying out a 10-minute test. The Table 6.2 shows the recorded frequency values.

Table 6.2: Maximum sampling frequency.

N_C	N_S	$f_{S_{max}}$ (Hz)
64	0	800
64	6	730
21	0	2160
21	6	1690
4	0	5970
4	6	3380
1	0	10300

The main limitation on the maximum attainable frequency is given by the time of acquisition of a *run* (*run* refers to the sampling of $N_C + N_S$ channels, the data of a *run* correspond to the same instant of time). For almost all system configurations it is used more than 90% of the time to acquire samples, leaving less than 10% to perform other tasks, mainly sending packages to the WiFi radio module. Therefore, a reduction of the acquisition time of a *run* would improve the maximum frequency currently reached by the system.

Battery run-time measurements

A test with this parameters: $N_C = 64$, $N_S = 0$ and $f_S = 770$ Hz, was left running until the battery could not maintain the minimum voltage required by the RHD2132 chips (3.2 V). The test lasted 24 hours and 22 minutes. This represent an average supply current of 139 mA.

[2]Acquisition time: time elapsed between the timer that controls the sampling frequency expires, and the sampled data is copied to the radio buffer.

Full-system test

At the inputs of the AFE, known signals were injected for different system configurations all with an amplitude of 10 mV_{pp}, and choosing $f_{low-pass} = 20$ kHz and $f_{high-pass} = 0.1$ Hz, and compared with the registered data. In Fig. 6.6 the signal is within the amplifier band-pass and an attenuation of 3.7% is observed (the amplitude of the signal is 9.63 mV_{pp}). This small attenuation can be explained by the fact that the input signal amplitude equals the maximum input linear range of the AFE, which is 10 mV_{pp}. Fig. 6.7 presents an actual EEG test.

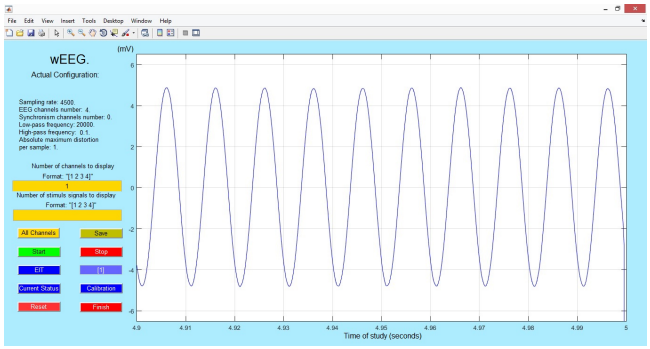


Figure 6.6: Input: sinusoid of 100 Hz.

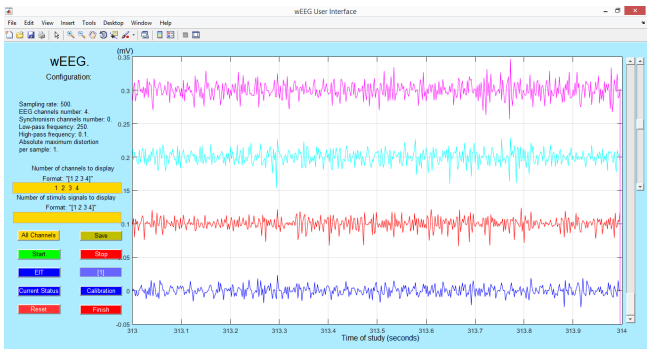


Figure 6.7: EEG test.

6.2.3 Conclusions

The wireless EEG recording system developed is capable of acquiring up to 64 EEG signals and 6 synchronization signals, with a programmable sampling frequency between 100 Hz and 10 kHz, and with an autonomy of more than 24 hours. The system supports four types of system configuration (1, 4, 21 or 64 channels), with a programmable band-pass filter where the high-pass frequency can vary between 0.1 Hz and 500 Hz and the low-pass frequency can vary between 100 Hz and 20 kHz. The maximum distance measured between the wireless module and the PC was 12 meters (but the system has the potential to operate in a greater range).

6.3 Wireless EEG recording system II: Bluetooh + data compression

As discussed in Section 2.5, data compression can be a key factor in a wireless biopotential recording system, not only for reducing power consumption, usually driven by the transmission [120], but also to overcome limitations of wireless technologies in the maximum data throughput that can be attained. For example, a EEG recording system with 64 channels, 16-bits per sample, at 1 ksps, requires a payload data rate of 1 Mbps, which is a throughput attainable by Bluetooth but not by other low-power transmission protocols such as IEEE 802.15.4. Moreover, common low-power transmission protocols available at this moment are unable to support 256 channels (payload data rate of 4 Mbps).

EEG data acquired for clinical purposes is often required to be processed, transmitted and stored without distortion; this establishes the need for lossless compression algorithms, in which the decompressed digital signal is identical to the originally captured one. If the preceding requirement is relaxed to allow a small, prescribed maximum per-sample distortion on the recovered signal, we arrive at the so called *near-lossless* setting. The near-lossless setting allows for significantly higher data rates and/or number of channels, with a user-controlled maximum sample reconstruction error given by a parameter δ. This configuration guarantees that the reconstructed value of each sample differs by up to δ quantization levels from the originally acquired sample.

The impact of EEG compression on the overall energy consumption of an electroencephalograph is driven by two factors that are generally opposed: the better the compression ratio, the more energy saved on transmission, but the more complex the compression algorithm, the greater the energy consumed in computing. [36] present two low-complexity EEG compression algorithms and evaluate this trade-off in actual hardware. These algorithms, which are inspired on the same statistical model as [1], both admit lossless and near-lossless variants, and are suitable to be implemented in a low-power hardware because they require only basic operations. In this Section we summarize the work reported in [36] (which is an extended version of [35]) focusing in the areas that we were more involved (hardware implementation and experimental work).

6.3.1 Low-power platform

The EEG low-power platform, depicted in Fig. 6.8, comprises an AFE, an ADC, a low-power processor (MCU), a BT radio transceiver and a power supply subsystem. All modules are powered by a 3.3 V dc source. The AFE and ADC stages, as well as the processor block, are exactly the same introduced in Section 6.2. The BT radio transceiver core is a module based on a CC2564 chip by TI. This is a dual mode module that supports Bluetooth 4.1 in low energy mode (BLE), and basic (BR) or enhanced data rate (EDR) mode. The prototype uses the EDR mode with serial port profile (SPP); this allows for high throughput configurations, e.g. 31 channels at 1 ksps/ch, which would not be affordable with BLE 4.1.

The processor embedded software is responsible for receiving the sample data, running the compression algorithm, and transmitting the compressor output to the BT module. A round-robin with interrupts architecture is adopted, where ISRs are extensively used to exchange (transmit and receive) data, and keep the processor in sleep mode while no processing is needed. The microcontroller's timer is used to trigger a new sample acquisition. The samples (one from each channel), received via the SPI interface, are stored in a input buffer. Once the input samples of all channels

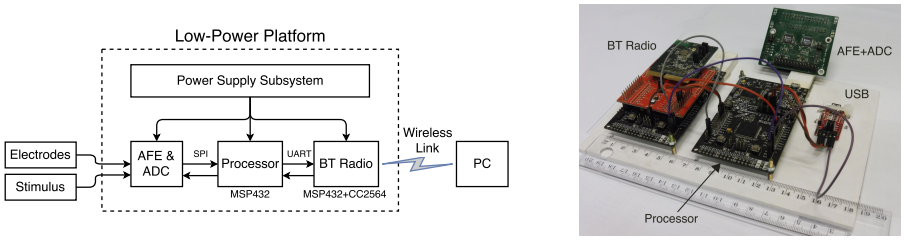


Figure 6.8: Bluetooth wireless EEG recording system.

are received, the compression algorithm is executed. The compressor output is stored in an output buffer to be transferred to the BT module through the UART interface. Once completed, the microcontroller enters in sleep mode.

In order to asses the platform using a controlled setup, the software module responsible for receiving the sample data from the RHD2132 chips via SPI is replaced by a Test Double. The Test Double module supplies data that is either received via a USB interface from a PC or directly read from the processor memory.

6.3.2 EEG Compression algorithms

The lossless, real time and low power requirements of the platform impose severe restrictions on the latency and computational resources of its embedded software. [1] reports a low-latency, low-complexity algorithm (the complexity actually grows linearly in storage and number of operations with respect to the number of channels), with controllable per-sample distortion. Thus, [36] choose [1] as the starting point; the algorithms developed involve non-trivial modifications of the original method with the goal of making it suitable for implementation on a low-power microcontroller with minimum computational and memory requirements.

As most EEG compression algorithms, the method in [1] exploits temporal and spatial sample correlations. These are induced by natural properties of the target signal such as temporal continuity, natural correlation of neural activity across regions, and spatial smoothing due to the different layers of tissue that separate the source signals (the neurons) from the point where they are measured (the electrodes). The essence of the algorithm is summarized below (see Fig. 6.9 and [1] for further details):

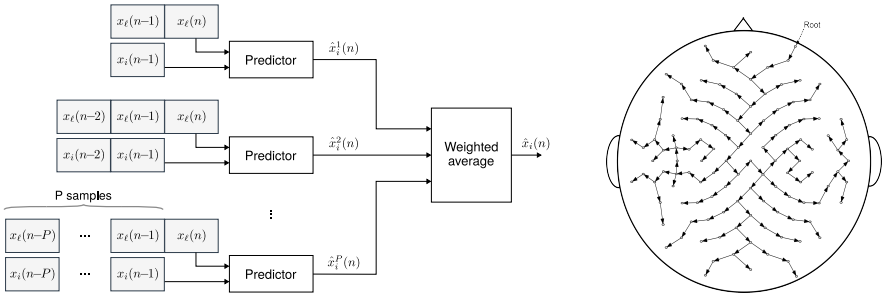


Figure 6.9: Compression algorithm of [1]. LEFT: block diagram of the prediction scheme; here $x_i(n)$ refers to the value of channel i at discrete time n, x_ℓ is the "helper" (parent) channel of x_i, P is the maximum order of the predictors, $\hat{x}_i^p$ is the p-th order prediction of x_i and $\hat{x}_i$ is the final prediction for that channel. RIGHT: sample tree used when deciding which channel helps which; the root channel is encoded with no help.

- The coding stage is predictive: both encoder and decoder predict the value of each sample from previously encoded samples; the actual value is described to the decoder by encoding the difference with respect to the prediction using the *Golomb-Rice code* [121].
- Channel samples are encoded in a pre-specified order following a tree; the root channel is predicted using past samples only, whereas all other channels have a *parent channel* (corresponding to their parent in the tree) that "helps" them, meaning that the past (and present) information about the parent channel is used for predicting the present sample of the child channel.
- Each sample prediction is a weighted average of a set of linear predictions of different orders, which are combined using an *exponential weighting* scheme [122] to form a final prediction.
- All these linear predictions are adaptive; they are updated in an online fashion using an efficient implementation of a multi-channel Recursive Least Squares (RLS) algorithm [123].

The performance and memory constraints of the target platform make the RLS algorithm used in [1] infeasible for high throughput scenarios and, in general, not very competitive in energy consumption. Instead, [36] use a multi-channel extension of a simple integer-based, adaptive, single-channel prediction algorithm originally proposed by Speck in [124]. This extension, is an original contribution of [36]. It turns out that although a compressor implemented with this predictor is significantly less complex, and thus requires a fraction of the resources, it still attains a performance similar to a floating-point RLS implementation (see Table 6.4 in Section 6.3.3). As an additional contribution, [36] propose an efficient integer implementation of the exponential weighting algorithm, which further improves the performance of the predictor. These tools, together with a cautious selection of a reduced set of predictors and other computation savings described in [36], result in a very simple and efficient compression algorithm that we refer to as MCS (Multi-Channel Speck). In addition, by replacing the adaptive predictors by fixed ones, [36] derives a significantly faster algorithm at the cost of some compression performance degradation, termed MCF (Multi-Channel Fixed). Finally, a near-lossless encoding scheme that applies to both MCS and MCF is also adopted.

6.3.3 System test

MCS and MCF algorithm were initially developed for a desktop computer and the source code later ported to the low-power platform and compiled with the GNU v4.8.4 (Linaro) compiler. For comparison purposes, a C implementation of the algorithm proposed in [1] (named FLO) was also ported and tested on the platform.

All the EEG signals used in the experiments reported are taken from publicly available databases:

- DB1a and DB1b [125, 126]: 64-channel, 160 Hz, 12 bits EEG of 109 subjects using the BCI2000 system. Recordings are divided in 2-minute motor imagery task (DB1a) and 1-minute calibration (DB1b).
- DB2a and DB2b [127] (BCI Competition III): 118-channel, 1 kHz, 16 bits EEG of 6 subjects performing motor imagery tasks (DB2a). DB2b is a 100 Hz downsampled version of DB2a.
- DB3 [128] (BCI Competition IV): 59-channel, 1 kHz, 16 bits EEG of 7 subjects performing motor imagery tasks.

- DB4 [129]: 31-channel, 1 kHz, 16 bits EEG of 15 subjects performing image classification and recognition tasks.

21, 31, and 59 channel EEG signals from databases DB2[3], DB4, and DB3, respectively, were used. EEG signals at 250 Hz and 500 Hz were obtained by downsampling the original data.

Power consumption

The power consumption of the AFE and ADC stages depends exclusively on the input data rate, i.e., the sampling frequency and number of channels. We thus focus on the power consumption of the processor block, which depends on the complexity of the compression algorithm, and on the power consumption of the BT radio block, which depends on the data rate output by the compressor.

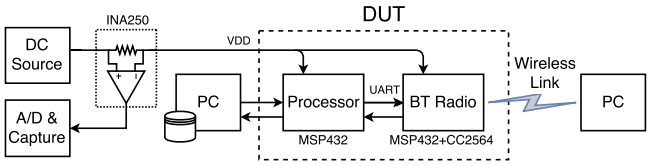


Figure 6.10: Current consumption and throughput measurement setup.

The setup used to measure the current consumption of both the processor and the BT radio is presented in Fig. 6.10. The data is fed to the platform via a USB interface from a PC, and the data rate is controlled by the combination of an internal timer of the processor and hardware flow control, used to signal the PC when a new sample can be received. Upon completing the compression of a vector sample the processor enters in sleep mode until the timer expires.

The power consumption of BT depends on the state of the link, which can be any of *idle*, *connected*, or *transmitting*. Fig. 6.11 shows measured samples of current consumption over time for each of these states; the curves are characteristic of BT communications [131].

BT links in *active* state (i.e., connected and transmitting states) require periodic exchanges of packets in order to keep the connection active and synchronized. These transmissions can be seen as the peaks in the plot of Fig. 6.11b; transmissions with actual payload can be seen as pulses in Fig. 6.11c. In *sniff mode*, the BT device transmits/receives only at certain regular time intervals and during a specific period. This allows the radio to enter a low-power mode between transmissions, which results in an energy saving in exchange for a smaller maximum attainable throughput and slightly larger latency. The power consumption in sniff mode for a sleep time period of 30 ms is shown in figures 6.11d and 6.11e; we notice a reduction in the number of current consumption peaks with respect to figures 6.11b and 6.11c. To evaluate the current consumption of the BT radio alone, we modify the setup of Fig. 6.10 by feeding the processor directly from the voltage source and measure the current drain.

Fig. 6.12 shows the current consumption of the BT radio for different configurations of sampling rate and number of channels, as a function of the data throughput, for both BT with sniff mode off and on. The figure also shows, in dashed lines, the plots of a linear regression for each of the sniff modes; we observe an excellent fit in both cases.

[3]We picked the channels that comprise the international 10-20 system [130].

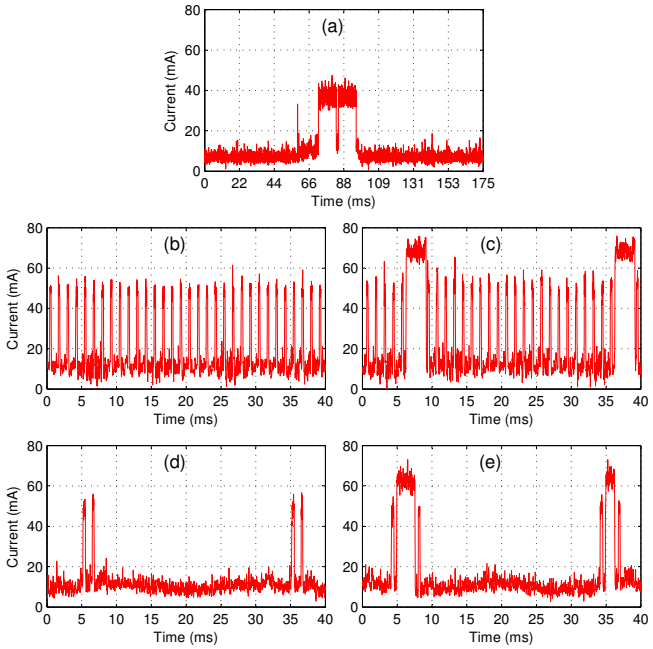


Figure 6.11: Current consumption vs. time for different Bluetooth transmission states measured in the low-power platform: (a) idle, (b) connected, (c) transmitting, (d) connected with sniff mode, and (e) transmitting with sniff mode.

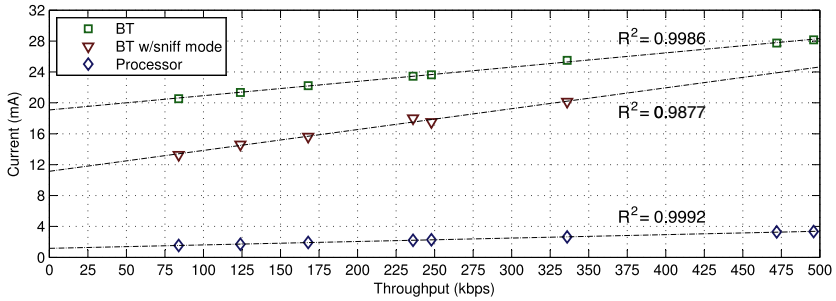


Figure 6.12: Current consumption vs. data rate, for processor (MCF, lossless compression) and BT.

Compression time and memory usage

The platform performance, in terms of processing time and memory usage, is detailed in Table 6.3 for MCS and MCF. Results indicate that MCF shows a speedup of 40–50% relative to MCS, and also a lower usage of RAM memory. On the other hand, the FLASH memory usage is nearly constant in all cases, 27.5 kB and 26.6 kB for MCS and MCF, respectively. Table 6.3 reports on the lossless versions of the compression algorithms ($\delta = 0$). The near-lossless versions ($\delta > 0$) do not increase the memory usage, and they increase the processing time by less than 3%.

Both MCS and MCF execute much faster than FLO, the average compression time per scalar sample (CTPS) of FLO is almost 10 times larger than that of MCS on the

Table 6.3: Platform performance depending on the compression algorithm version ($\delta = 0$).

Alg.	Number of channels	Proc. time per sample (ms)	Max. sampling rate (sps)	RAM usage (kB)
MCS	21	0.432	2313	11.7
MCS	31	0.593	1686	14.8
MCS	59	1.232	812	23.4
MCF	21	0.286	3496	8.6
MCF	31	0.418	2394	10.1
MCF	59	0.826	1211	14.4

low-power platform (see Table 6.4).

Compression performance

For each database, each data file was compressed separately and the overall compression ratio (CR), in bits per sample, was calculated as L/N_s, where N_s is the sum of the number of scalar samples over all files of the database, and L is the sum of the number of bits over all compressed files of the database; *smaller* CRs are better.

Table 6.4: Compression ratio in bits per sample (smaller is better) of MCS, MCF algorithms for different databases ($\delta = 0$) and average CTPS (μs). Comparison with state-of-the-art.

Algorithm	DB1a	DB1b	DB2a	DB2b	DB3	DB4	CTPS
MCS	4.82	4.94	5.34	6.97	5.47	3.81	0.08
MCF	5.09	5.18	5.96	7.41	5.90	4.35	0.05
FLO	4.74	4.82	5.30	6.98	5.46	3.64	0.51
[1]	4.70	4.79	5.21	6.93	5.42	3.58	0.92
[132]	5.37	5.45	5.69	7.69	5.99	3.73	1.07

Table 6.4 shows the CRs and average CTPSs of MCS and MCF compared to those of FLO, those reported in [1], and those obtained for ALS (MPEG-4 audio lossless coding standard [132], ALS attains the best CRs in [132–135] for the same databases). MCS shows CRs that are very similar for some databases and slightly higher (worse) than those of FLO in some cases. This deterioration is expected, due to the various simplifications made to lower the complexity of MCS. A compression performance deterioration is also observed in MCF with respect to MCS, due to the use of fixed predictors instead of adaptive ones, which, on the other hand, yielded important reductions in memory and time requirements. Notice, however, that the performance of MCF is still superior to that of the best algorithm reported in [132–135] for all the databases except DB4. Comparing the CR of MCS with the original sample resolution for each database we observe that the amount of data that needs to be transmitted is reduced by a factor of at least 2.3 times, for DB2b, and up to 4.2 times, for DB4. Finally, Table 6.5 shows results for the near-lossless versions.

Power consumption vs. throughput

Fig. 6.13 shows the current consumption of the platform (compression plus transmission) as a function of the data throughput for several values of the distortion parameter δ (shown next to the curve), different sampling rates (different color lines), and different number of channels (different markers). The curves on top correspond to BT with

Table 6.5: Compression ratio (bits per sample) of MCS and MCF algorithms for different databases (smaller is better).

	δ	DB1a	DB1b	DB2a	DB2b	DB3	DB4
MCS	0	4.82	4.94	5.34	6.97	5.47	3.81
MCS	2	2.79	2.86	3.23	4.66	3.35	2.30
MCS	5	2.04	2.08	2.37	3.57	2.45	1.83
MCS	10	1.62	1.64	1.86	2.75	1.91	1.58
MCF	0	5.09	5.18	5.96	7.41	5.90	4.35
MCF	2	3.03	3.06	3.70	5.10	3.66	2.53
MCF	5	2.27	2.26	2.73	3.94	2.70	1.98
MCF	10	1.82	1.81	2.08	3.10	2.08	1.67

sniff mode off and the ones on the bottom to BT with sniff mode on. Fig. 6.13a shows the results for MCS and Fig. 6.13b for MCF. The dashed lines represent the current consumption of the BT radio alone transmitting raw (uncompressed) data.

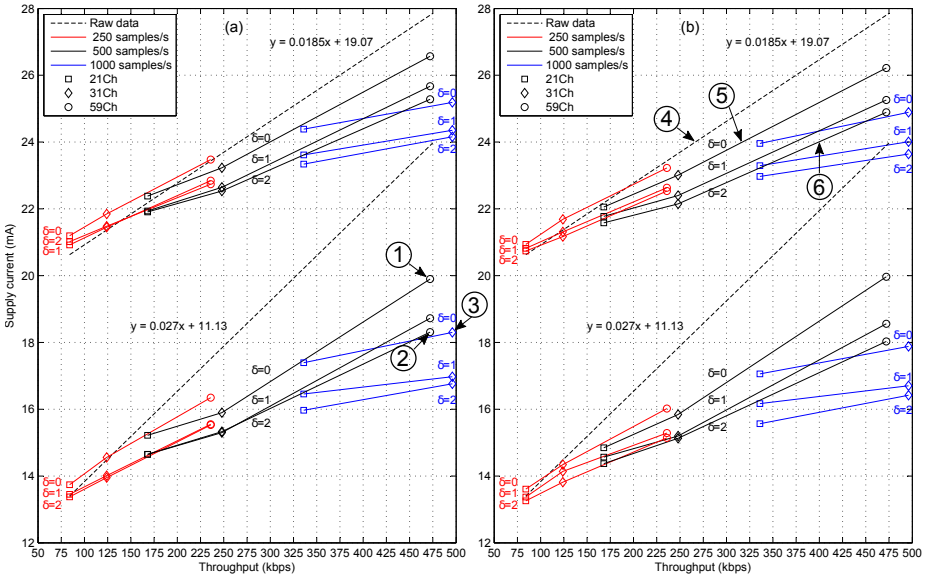


Figure 6.13: Current consumption vs. throughput. (a) MCS, BT (top) and BT with sniff mode on (bottom). (b) MCF, BT (top) and BT with sniff mode on (bottom). The dashed line represents the current consumption as a function of the *uncompressed* data throughput.

We observe that the proposed low-power platform is able to perform lossless compression of a 59-channel acquisition at a rate of 500 sps/ch, with a current consumption of 19.9 mA, that is 337 μA per channel (marked as 1 in Fig. 6.13). Using near-lossless compression with distortion $\delta = 2$, in the same setting, results in almost 10% reduction in current consumption (marked as 2 in Fig. 6.13). On the other hand, for 31 channels, a sampling rate of 1000 sps/ch can be attained with a consumption of 590 μA/ch (marked as 3 in Fig. 6.13).

Fig. 6.13 illustrates the trade-off between power invested in compression and power saved in data transmission. For very low data rates compressing does not pay off. For larger throughputs, however, the savings in transmission exceed the cost of compres-

sion, resulting in a reduction of up to 10% in current consumption.

The experiment also shows that, for a given current consumption, the proposed compression scheme results in a substantial increase in the maximum attainable throughput. For example, a budget of 24 mA allows for an uncompressed throughput of 265 kbps (see 4 in Fig. 6.13), while the use of the MCF algorithm allows for throughputs of up to approximately 315 kbps for $\delta = 0$ (marked as 5 in Fig. 6.13) and 400 kbps for $\delta = 2$ (marked as 6 in Fig. 6.13). In other words, using data compression we obtain an increase in throughput of 19% with the lossless setting and 51% with the near-lossless one.

6.3.4 Conclusions

We have presented a successful implementation, in a low-power wireless platform, of two lossless/near-lossless multichannel EEG compression algorithms that offer different levels of complexity and compression performance. We used these implementations to experimentally evaluate, the energy saving and the increment in attainable throughput derived from the reduction in the amount of data transmitted; these turn out to be very significant for large throughput scenarios.

Future work includes evaluating the low-power platform with other physiological signals such as ECG, for which the proposed compression algorithm yields very promising results [1]. Another future objective is to develop a custom SoC using one of the proposed algorithms to further reduce power consumption.

6.4 Comparison and conclusions

In order to extend the field of application of traditional electrophysiology, wireless biopotential recording systems must allow the test subject to move freely for a reasonable time (about one day) within a reasonable area (about ten meters).

There were and there are multiple efforts on this direction. For example [136, 137] present systems that attain very low power consumptions using very specialized custom hardware, and at the expense of other features we designed for, such as transmission range, robust and secure transmission protocols and compatibility with a wide range of devices. On the other hand, there are reaserch works such as [138, 139] where systems based on standard hardware are presented. In addition, there are several commercial systems [90–92, 140]. A comparison of these implementations with our systems is presented at the end of this section.

This Chapter presented three experiences where we designed and implemented prototypes of biopotential wireless recording systems based on off-the-shelf components. In Table 6.6 we summarizes its performance.

Table 6.6: Wireless biopotential recording systems described in Chapter 6.

System	[33]	[34]	[36]-MCS
Number of channels	4	64	59
Autonomy (hours)	109	>24	156
Average supply current (mA)	31.2	139	21.7
Effective data rate (ksps/ch)	2.5	0.8	0.5
Input-referred noise (nV/$\sqrt{Hz}$)	11	21	21
Comm. protocol	TI propietary	WiFi	BT (snif mode)
Application	Neural	EEG	EEG

Firstly [33], which is focused on neural signal recording, has 4 channels and the AFE was built with low-cost discrete components. It has a TI low power communication protocol with limited data throughput (10 ksps). The autonomy is excellent (109 hours powered from a 3400 mAh Li-Ion battery). The implementation of the PCB of the AFE suffers from severe problems of interference from the radio block.

Secondly [34], that is focused on EEG signal recording, has 64 channels and the AFE was implemented with an off-the-shelf integrated circuit. The communication protocol is a high data rate standard (WiFi) which is not low power. This is traduced in an excellent range of work (greater than 12 meters) and an acceptable autonomy (24 hours powered from a 3400 mAh Li-Ion battery). The effective maximum data rate (64 ch x 800 sps/ch = 51 ksps) can be largely increased. The current bottleneck is in the data processing block: the 16-bit SPI communication between the RHD2132 chips and the MCU takes about 1 ms for acquiring 64 channels. A possible way to decrease this time is to use the DMA (Direct Memory Access) peripheral of the MCU. Another possible way is to change the MCU. However, to the best of our knowledge, the MSP432 is the best option to balance low power and processing capabilities. Thanks to the care put into the AFE design, there were no problems of interference between the analog part of the circuit and the radio frequency components.

Finally [36], which is focused on EEG signal recording, has 59 channels and the AFE was implemented with an off-the-shelf integrated circuit. The communication protocol is standard (BT) and a data compression scheme is introduced. The autonomy is excellent (156 hours powered from a 3400 mAh Li-Ion battery). The effective maximum data rate was not measured, but was close to 59 ksps (59 ch x 1 ksps/ch). The bottleneck was simultaneously in the data processing block and the data communication block. At the processing block, the compression algorithm requires more than 1 ms in the MCS version and 0.828 ms in the MCF version, to process 64 channels. In the latter we almost achieved 1 ksps/ch. However, at this rate, the data communication block starts to fail, a 944 kbps effective data rate is beyond the Bluetooth 4.1 radio module capabilities (59 ch x 1 ksps/ch x 16 bits = 944 kbps). Future work should include changing the radio module for a Bluetooth 5 (released in June 2016) module aiming to achieve a higher effective maximum data rate.

Comparing commercial systems with research implementations pose some difficulties. For example, Table 6.7 shows that our systems are lighter, and achieve longer autonomy than available commercial systems. However, there are various constraints, such as regulatory requirements, packaging and aesthetics, and use of mature technologies, among others, that apply to commercial systems but not to research prototypes. Additionally, some important parameters of commercial systems are often not reported on, which limits the scope of the comparisons. Therefore, head-to-head comparisons with commercial systems may be regarded as incomplete. On the other hand, with the previous disclaimer on mind, it can be useful to perform the comparison. Table 6.7 shows a comparison between our EEG systems and some selected commercial EEG recording devices and research implementations built with off-the-shelf components. It is observed that our system compares favorably, being the only solutions that offers the acquisition of a high number of channels with an autonomy greater than 24 hours.

Undoubtedly there is room to keep improving. There are improvements that will come from advances in known technologies, and others will come from new technologies. For example, the increase of the processing capacity of low power MCUs and/or the increase of effective data rates of standard protocols. Other improvements will come from merging these standard technologies with our own developments. Part of our future work is to implement a wireless multi-channel recording system, based on the AFE architecture presented in Chapter 5, and on one of the systems presented in this chapter. We believe that we are really close to develop a 64-channel 1 ksps/ch

wireless biopotential recording system that can continuously operate for more than one week.

Table 6.7: EEG wireless recording systems comparison.

System	wEEG I	wEEG II - MCS	Nicolet	g.Mobilab+	eego rt	HD-72	NIRS-EEG
Number of channels	64	59	64	8	64	64	8
Weight (grams)	270	270	800	360	500	350	800
Autonomy (hours)	>24	156	12-24	25-100	5	6	33
Effective data rate (ksps/ch)	0.8	0.5	4	0.256	2	0.5	0.32
Input-referred noise	$2.4\mu V_{rms}$	$2.4\mu V_{rms}$	2μ V_{pp}	N/A	$1\mu V_{rms}$	$0.7\mu V_{rms}$	N/A
Comm. protocol	WiFi	BT	WiFi	BT	WiFi	BT	BT
Manufacturer	-	-	Natus	g.tec	ANT Neuro	Cognionics	-
Reference	[34]	[36]	[90]	[91]	[92]	[140]	[139]

Chapter 7

Conclusions

This thesis introduced a novel integrated DDA-based preamplifier architecture targeting CMRR sensitive neural recording applications, including silicon implementation, experimental characterization and in-vivo validation. The architecture was presented and analyzed in depth, deriving the preamplifier transfer function and the main design equations. The design flow and the main design trade-offs were discussed. In addition, we presented the detailed analysis of a technique for blocking the input dc component and setting the high-pass frequency without MOS pseudo-resistors.

A fully-integrated neural preamplifier, that performs well in line with the state-of-the-art of the field while providing enhanced CMRR performance, was fabricated in a 0.5 μm CMOS process. Results from measurements show that the gain is 49.5 dB, the bandwidth ranges from 13 Hz to 9.8 kHz, the CMRR is very high (greater than 87 dB), and it is achieved jointly with a remarkable low noise (1.88 μV_{rms}) and current-efficiency (NEF = 2.1). To the best of our knowledge, this preamplifier is the best option for applications that simultaneously need low noise, high CMRR and current-efficiency. A second version of the preamplifier with one external capacitor achieves a high-pass frequency of 0.1 Hz while keeping the performance of the fully-integrated version.

We presented in-vivo measurements made with the proposed architecture in a weakly electric fish (*Gymnotus omarorum*), showing the ability of the amplifier to acquire neural signals from high amplitude common mode interference in an unshielded environment. This was the first in-vivo testing of a neural recording integrated circuit designed in Uruguay done in a local lab. Furthermore, signals recorded with our unshielded low-power battery-powered preamplifier perfectly match with those recorded with a shielded commercially available amplifier (ac-plugged, without power restrictions). The proposed preamplifier has proved to be very appropriate for in-vivo recording of LFPs and unitary signals from the brain stem of a weakly electric fish.

In this thesis we extended and applied the previously mentioned architecture to band-pass biquad filters (specially but not only to those with differential input). Firstly, we showed that traditional implementations of these filters require an OTA devoted to establish the high-pass characteristic and block the dc input (which implies an overhead in terms of power consumption and silicon area). Secondly, we derived the equation that rules the trade-off between the power consumption of these filters and its capacity of blocking large dc inputs. Then, we proposed, among other changes, to replace the aforementioned additional OTA with our circuit for blocking the input dc component and setting the high-pass frequency.

Two filters that meet the same requirements were designed and compared, while

the first was based on our novel approach, the second was based on a traditional implementation. The novel architecture presents, as the traditional approach does, a trade-off between gain and dc input blocking capacity. In our approach the loss of gain is greater than in the traditional approach, but it is remarkable that our implementation does not lose the high-pass characteristic for high dc input values while the traditional one does. Our architecture avoids the overhead in terms of power consumption and silicon area that traditional approaches introduce for establishing the high-pass characteristic and to block the dc input. This feature enables to decrease the power consumption, or to increase the levels of dc input to be blocked without jeopardizing the power consumption. Results from Monte Carlo simulations show that the proposed architecture, compared with a traditional one, presents a 30 % reduction in power consumption and more than doubles the dc input that can be blocked. A comparison with state-of-the-art filters shows that our approach is an efficient way to balance the trade-off between a reasonable precision in setting the high-pass frequency, high CMRR and dc input signal blocking capacity.

This thesis introduced a novel integrated programmable AFE architecture formed by the preamplifier presented in Chapter 3 and two additional band-pass amplifying stages based on the filter architecture presented in Chapter 4. Firstly, the main design trade-offs (noise versus power, gain versus power, noise versus gain, linearity versus gain, among others) of the proposed architecture were discussed and their impacts in the design of the processing chain in terms of assignment of gain, noise, power consumption, linearity and programmability to each stage were shown. Noise is the most critical requirement of the first stage because ultra-low-amplitude signals must be amplified and filtered. Therefore, the noise-power trade-off, expressed in terms of the NEF, led us to assign most of the power budget to the first stage. Furthermore, the noise-gain trade-off and linearity-gain trade-off determined the gains of the first and second stage. Moreover, it was shown that programming wide ranges of gain and/or cut-off frequencies implies wide ranges of transconductance values and high capacitor values.

The proposed front-end architecture is focused in acquiring a wide range of physiological signals. This can be done because the gain is programmable between 57 dB and 99 dB, the low-pass frequency is programmable between 116 Hz and 5.2 kHz, and the high-pass frequency is 0.1 Hz, while the maximum power consumption of the front-end is 11.2 μA and its maximum equivalent input-referred noise voltage is 1.87 μV_{rms}. The comparison between our front-end and other works in the state-of-the-art shows that our front-end presents the best results in terms of CMRR and noise, has the greatest value of gain and equals the best NEF reported.

On our way to designing a system based on the previously proposed circuits, we developed three prototypes of biopotential signals acquisition systems based on off-the-shelf components. Firstly, a wireless neural recording system based on a MSP430 SoC from TI was implemented. The system is capable of recording up to 10 ksps from up to 4 channels. The wireless communication achieved a remarkable throughput of 358 kbps with a packet loss of less than 2% (without retransmissions) at 10 dBm transmit power, within a 5 meters range. The wireless module powered with two AAA batteries (900mAh) can operate for more than 28 hours. Secondly, a wireless EEG recording system based on two RHD-2132 analog-front-end from Intan Technologies, a MSP432 microcontroller and a WiFi radio module from TI was developed. The system is capable of acquiring up to 64 EEG signals and 6 synchronism signals at 800 sps for more than 24 hours, powered from a 3400 mAh Li-Ion battery. The maximum distance measured between the wireless module and the PC was 12 meters. Finally, a wireless EEG recording system based on two RHD-2132 analog-front-end, a MSP432 microcontroller and a Bluetooth radio module from TI was implemented. Two novel,

low-complexity, efficient compression algorithms were ported and tested in this low power platform. These algorithms were tested on six public EEG databases comparing favorably with the best compression rates reported up to date in the literature. The system is capable of acquiring up to 64 EEG signals at 500 sps for 156 hours powered from a 3400 mAh Li-Ion battery.

7.1 Thesis contributions

As a summary of the previous section, the following paragraphs will highlight the main contributions of this thesis:

- We introduced a DDA-based **current-efficient preamplifier architecture for CMRR sensitive neural recording applications**, including silicon implementation and experimental characterization.
- The measured neural preamplifier exhibits an overall **state-of-the-art performance and enhanced CMRR**.
- We presented the detailed analysis of a **technique for blocking the input dc component and setting the high-pass frequency** without jeopardizing power consumption.
- We introduced a **band-pass biquad filter architecture** that provides a significant reduction of power consumption and/or makes it possible to block higher levels of dc at the input (without using decoupling capacitors).
- We proposed, designed and simulated an **integrated programmable analog front-end architecture** with a performance well in line with the state-of-the-art in the field.
- Some system-level topics were addressed during the thesis, including the design and implementation of three prototypes of **end-to-end wireless biopotentials recording systems** based on off-the-shelf components. In one of these systems, we participated in the implementation, characterization and testing of two novel, low-complexity, **EEG compression algorithms**.
- We performed the **first in-vivo testing of a neural recording integrated circuit designed in Uruguay done in a local lab.**

7.2 Future work

In the years to come, neuroscience research will heavily depend on multi-unitary recording performed in parallel to behavior analysis. The development of a wearable, wireless, multi-channel and small device offering the user a synchronism mechanism, allowing the correlation between neural activity, sensory images, and behavior signals recorded by other devices, is a problem still not fully solved. Event related potentials and unit firing probability after sensory stimulus and before motor actions are currently recorded in neurosciences, medicine and psychology, among others disciplines. In the case of event related potentials, increasing the number of channels with small size and low power consumption would improve the possibility of source reconstruction. Large-scale multi-unitary recordings will allow scientists to search for correlations between the activities of neurons belonging to the same local circuitry and deciphering their functional connectivity and also to evaluate the effects on other brain regions through long connections. Peripheral studies, as for example Holter recordings of heart or skeletal muscle activities in medicine and sports, would benefit from the same type of

recording devices and simultaneous synchronous monitoring of physical activity. Finally, concerning EEG, an important challenge is electrode development. The use of dry electrodes will continue to grow boosted by applications in Brain-machine interface, wearable devices and Internet of Things, among others. This will push further the research on optimization methods for electrodes and signal acquisition circuits to alleviate the disadvantages of dry electrodes.

In this context, we expect that the present thesis is the first step to continue contributing in the followings areas:

Integrated neural acquisition:

- A high ICMR implementation of the proposed architecture was fabricated in a 0.5 μm process and is currently under testing. Some preliminary results were reported in [141] and we made them available in Appendix D.
- A low voltage (1.2 V) variant of the proposed architecture was fabricated in a 130 nm process and is currently under testing. This was done in the framework of an undergraduate thesis [108].
- If a large number of channels is required, it can be necessary to explore changes to the preamplifier architecture in order to reduce area. Firstly, smaller input transistors of Gm1 can be adopted (at the expense of increasing noise). Secondly, in order to reduce the area of integrated capacitors or avoid external capacitors, smaller OTAs can be implemented (for instance in [105] a 33 pS OTA is reported).
- Explore the possibility of modifying α to program or tune the preamplifier gain.
- New applications of the architecture can be explored, for instance in fully-differential filters and amplifiers.
- Implement a wireless multi-channel recording system, based on the AFE architecture presented in Chapter 5, and on one of the systems presented in Chapter 6.

On-chip processing:

- Spike detection (which can be made in the same chip of the AFE, or at the microcontroller level).
- Develop a custom integrated circuit using one of the compression algorithms in Chapter 6 to further reduce power consumption. The algorithm admits lossless and near-lossless variants, and requires only basic operations, which can be readily implemented using discrete logic blocks as part of a custom SoC.
- Conduct in-vivo tests/trials using the presented compression algorithms. Particularly, the near-lossless versions.

System level:

- Development of technological tools or platforms to study the behavior of living beings. For example, in order to asses the response of the animal, it is possible to conceive a system that allows to modify the impedance in a certain place of the water while performing a weakly electric fish neural recording.
- Development of technological tools or platforms to study and control cognitive processes. For instance, a platform that while performing a neural recording has the possibility of stimulate.

- An important part of the work presented in this thesis was performed in a multidisciplinary environment. The specifications, the evaluation of the trade-offs, the most important design decisions were made in close contact with neuroscientists. In addition, it was rewarding to work together with colleges from signal processing and information theory area. Future work should remain in this way.

7.3 Publications associated with the thesis

7.3.1 Journals

- **Julián Oreggioni**, Angel A. Caputi, and Fernando Silveira. *Current efficient preamplifier architecture for CMRR sensitive neural recording applications.* IEEE Transaction on Biomedical Circuits and Systems, 2018 [28].
- **Julián Oreggioni**, Pablo Castro-Lisboa, and Fernando Silveira. *Relaxing the maximum dc input amplitude vs. consumption trade-off in differential-input band-pass biquad filters.* International Journal of Circuit Theory and Applications, volume 44, number 9, pages 1706-1716, Sept. 2016 [30].
- Guillermo Dufort y Álvarez, Federico Favaro, Federico Lecumberry, Álvaro Martín, Juan P. Oliver, **Julián Oreggioni**, Ignacio Ramírez, Gadiel Seroussi, and Leonardo Steinfeld. *Wireless EEG System Achieving High Throughput and Reduced Energy Consumption Through Lossless and Near-Lossless Compression.* IEEE Transaction on Biomedical Circuits and Systems, volume 12, number 1, pages 231-241, Feb. 2018 [36].

7.3.2 Encyclopedia

- **Julián Oreggioni**, Angel A. Caputi, and Fernando Silveira. *Biopotential monitoring.* In Reference Module in Biomedical Sciences, Elsevier, 2017 [27].

7.3.3 Conferences

- **Julián Oreggioni**, and Fernando Silveira. *Integrated programmable analog front-end architecture for physiological signal acquisition.* Proceedings of IEEE International Instrumentation and Measurement Technology Conference (I2MTC), pages 108-112, May. 2014 [31].
- **Julián Oreggioni**, and Fernando Silveira. *Improving CMRR and NEF in neural preamplifiers.* IEEE 38th Annual International Conference of the Engineering in Medicine and Biology Society (EMBC), Late Breaking Research, Poster, Aug. 2016 [141].
- Fernando Silveira, **Julián Oreggioni**, and Pablo Castro-Lisboa. *Constraints and design approaches in analog ICs for implantable medical devices.* Proceedings of International Symposium on VLSI Design, Automation and Test (VLSI-DAT), pages 1-4, Apr. 2015 [29].
- Martín Causa, Franco La Paz, Santiago Radi, Juan P. Oliver, Leonardo Steinfeld, and **Julián Oreggioni**. *A 64-channel wireless EEG recording system for wearable applications.* Accepted to IEEE Latin American Simposium on Circuit and Systems (LASCAS), Feb. 2018 [34].
- Guillermo Dufort y Álvarez, Federico Favaro, Federico Lecumberry, Álvaro Martín, Juan P. Oliver, **Julián Oreggioni**, Ignacio Ramírez, Gadiel Seroussi, and Leonardo Steinfeld. *Wearable EEG via lossless compression.* Proceedings of

IEEE 38th Annual International Conference of the Engineering in Medicine and Biology Society (EMBC), pages 1995-1998, Aug. 2016 [35].

- Esteban Cilleruelo, Andrés Nacelle, Gerardo Robert, **Julián Oreggioni**, Fernando Silveira, and Angel A. Caputi. *Wireless Biopotential Signals Acquisition System*. Proceedings of Fourth Argentine Symposium and Conference on Embedded Systems (SASE/CASE), pages 1-5, Aug. 2013 [33].

7.4 Publications non associated with the thesis

7.4.1 Journals

- Leonardo Steinfeld, **Julián Oreggioni**, Diego A. Bouvier, Carlos A. Fernández and Jorge Villaverde. *Smart coulomb counter for self-metering wireless sensor nodes consumption*. Journal of Low Power Electronics, Volume 11, Number 2, pages 236-248, Jun. 2015

7.4.2 Conferences

- Javier Schandy, **Julián Oreggioni**, and Leonardo Steinfeld. *DC-DC switching converter as on-field self energy meter*. Proceedings of IEEE 7th Latin American Symposium on Circuits and Systems (LASCAS), pages 139-142, Feb. 28 - Mar. 2, 2016.
- Jorge Villaverde, Leonardo Steinfeld, **Julián Oreggioni**, Diego A. Bouvier and Carlos A. Fernández. *Self-energy meter in duty-cycle battery operated sensor node*. Proceedings of IEEE International Instrumentation and Measurement Technology Conference (I2MTC), pages 1595-1599, May. 2014.
- Carlos A. Fernández, Diego A. Bouvier, Jorge Villaverde, Leonardo Steinfeld and **Julián Oreggioni**. *Low-Power Self-Energy Meter for Wireless Sensor Network*. Proceedings of the IEEE International Conference on Distributed Computing in Sensor Systems (DCOSS), page 315-317, 2013.

Appendix A

Deduction of the architecture transfer function

Consider the small-signal operation of the circuit[1] of Fig. A.1. Applying superposition we will find i_{out1}:

$$i_{out1} = -i_{d7} + i_{d8} \tag{A.1}$$

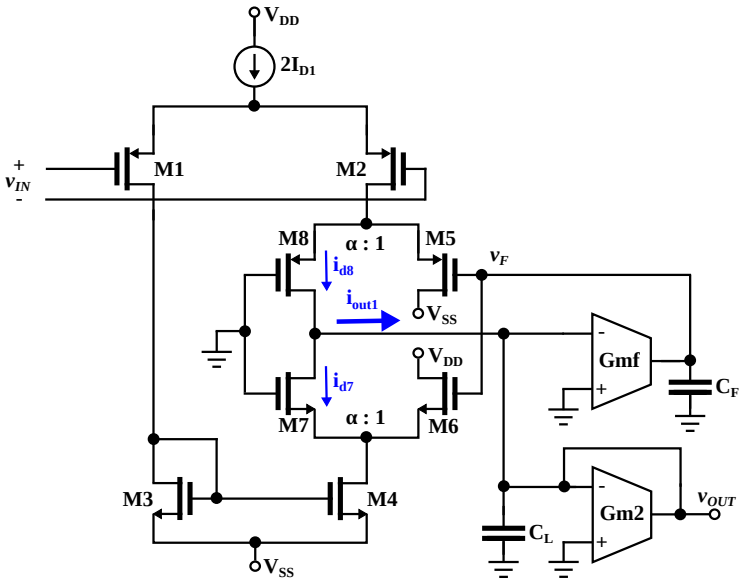


Figure A.1: Architecture.

Firstly, let us consider $v_F = 0$. v_{in} is applied to the M1-M2 input differential pair, therefore a current of $\frac{1}{2} g_{m1} v_{in}$ enters to the source of M5 and M8 while the same (with opposite sign) is copied by the mirror M3-M4 entering the source of M6 and M7. Fig. A.2 shows the small signal equivalent circuit.

[1] We assume that the Early voltage $V_A = \infty$ and $g_{mbs} = 0$.

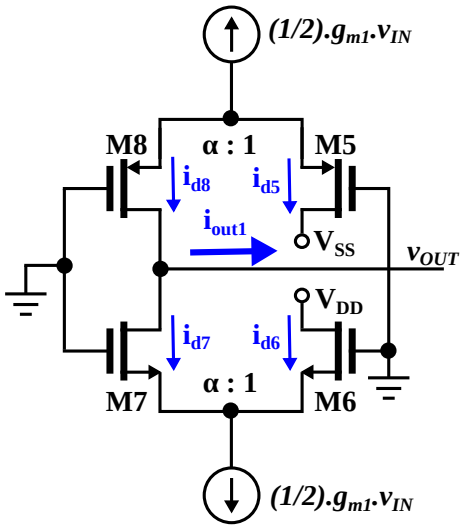


Figure A.2: Gm1 small-signal equivalent circuit with $v_F = 0$.

Due to the circuit symmetry is enough to study only one half. For instance, lets consider the upper half, where the M5 and M8 drain current are:

$$i_{d8} = -g_{m8} v_{s5,8} \tag{A.2}$$

$$i_{d5} = -g_{m5} v_{s5,8} \tag{A.3}$$

Applying Kirchhoff's current law (KCL) to the source of M5 and M8 we have:

$$-\frac{1}{2} g_{m1} v_{in} = -g_{m8} v_{s5,8} - g_{m5} v_{s5,8} = -(g_{m5} + g_{m8}) v_{s5,8} \tag{A.4}$$

Combining the previous two equations:

$$i_{d8} = \frac{1}{2} \frac{g_{m1} g_{m8}}{g_{m5} + g_{m8}} v_{in} \tag{A.5}$$

Analogously:

$$i_{d7} = -\frac{1}{2} \frac{g_{m1} g_{m7}}{g_{m6} + g_{m7}} v_{in} \tag{A.6}$$

Substituting the two last equations in Eq. A.1 yields to:

$$i_{out1} = \frac{1}{2} g_{m1} \left(\frac{g_{m8}}{g_{m5} + g_{m8}} + \frac{g_{m7}}{g_{m6} + g_{m7}} \right) v_{in} \tag{A.7}$$

Secondly, let us consider $v_{in} = 0$. In this case, no ac current flow through M1, M2, M3 and M4, therefore is enough to study the circuit depicted in Fig. A.3. Applying KCL in the output node we have:

$$i_{out1} = g_{m8} v_{s5,8} + g_{m7} v_{s6,7} \tag{A.8}$$

It can be seen that:

$$v_{s6,7} = \frac{g_{m6}}{g_{m7} + g_{m6}} v_F \tag{A.9}$$

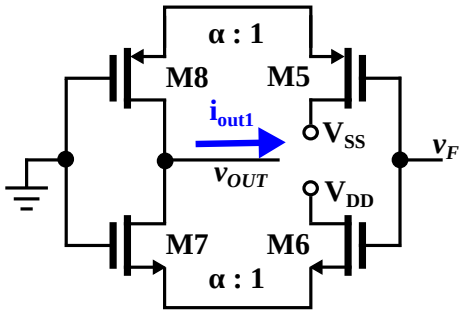


Figure A.3: Gm1 small-signal equivalent circuit with $v_{in} = 0$.

$$v_{s5,8} = \frac{g_{m5}}{g_{m5} + g_{m8}} v_F \tag{A.10}$$

Then, combining the previous three equations we have:

$$i_{out1} = \left(\frac{g_{m5} g_{m8}}{g_{m5} + g_{m8}} + \frac{g_{m6} g_{m7}}{g_{m7} + g_{m6}} \right) v_F \tag{A.11}$$

Therefore, applying superposition and thus substituting Eq. A.7 and Eq. A.11 in Eq. A.1 we arrive to:

$$i_{out1} = \frac{1}{2} g_{m1} \left(\frac{g_{m8}}{g_{m5} + g_{m8}} + \frac{g_{m7}}{g_{m6} + g_{m7}} \right) v_{in} + \left(\frac{g_{m5} g_{m8}}{g_{m5} + g_{m8}} + \frac{g_{m6} g_{m7}}{g_{m7} + g_{m6}} \right) v_F \tag{A.12}$$

Applying KCL in the node of v_f (see Fig. A.1) we have:

$$\frac{v_F}{v_{out}} = -\frac{G_{mf}}{sC_F} \tag{A.13}$$

Applying KCL in the output node v_{out} (see Fig. A.1) lead to:

$$i_{out1} = G_{m2} v_{out} + sC_L v_{out} \tag{A.14}$$

Then, combining the previous three equations with $G_{m1} = g_{m1}$, we have:

$$\frac{v_{out}}{v_{in}} = \frac{\frac{1}{2} \frac{G_{m1}}{C_L} \left(\frac{g_{m8}}{g_{m5} + g_{m8}} + \frac{g_{m7}}{g_{m6} + g_{m7}} \right) s}{s^2 + \frac{G_{m2}}{C_L} s + \left(\frac{g_{m5} g_{m8}}{g_{m5} + g_{m8}} + \frac{g_{m6} g_{m7}}{g_{m6} + g_{m7}} \right) \frac{G_{mf}}{C_L C_F}} \tag{A.15}$$

this equation analytically shows that the less current M5 and M6 drain, the greater the output current and the gain would be. In addition, the equation shows that taking $g_{m7} \gg g_{m6}$ y $g_{m8} \gg g_{m5}$ the gain can be doubled without affecting the overall performance. On the other hand, it is possible to design M7 and M8 to have $g_{m7} = g_{m8}$. Taking these two simplifications we arrive to the architecture transfer function:

$$\frac{v_{out}}{v_{in}} = \frac{\frac{G_{m1}}{C_L} s}{s^2 + \frac{G_{m2}}{C_L} s + \frac{(g_{m5} + g_{m6}) G_{mf}}{C_L C_F}} \tag{3.2}$$

It is simple to see than this function has a band-pass characteristic, where the low-pass frequency $f_{low-pass}$ is given by Eq. 3.3, the band-pass gain G by Eq. 3.4 and the high-pass frequency $f_{high-pass}$ by Eq. 3.5:

$$f_{low-pass} = \frac{G_{m2}}{2\pi C_L} \tag{3.3}$$

Appendix A. Deduction of the architecture transfer function

$$G = \frac{G_{m1}}{G_{m2}} \tag{3.4}$$

$$f_{high-pass} = \frac{g_{m5} + g_{m6}}{G_{m2}} \frac{G_{mf}}{2\pi C_F} \tag{3.5}$$

Appendix B

Architecture linearity

If we consider M6-M7 and M5-M8 as differential pairs, they potentially can introduce a multiplication effect between v_{in} and v_F. Next, we made the calculations that yields to the following conditions:

$$v_{in} \ll \frac{2}{(g_m/I_D)_1} \tag{B.1}$$

$$v_F \ll \frac{2\alpha}{(g_m/I_D)_{C1}} - \alpha n U_T \tag{B.2}$$

Considering that M1, M2, M5, M6, M7 and M8 are in weak inversion and $\alpha = 100$, the conditions are fulfilled:

$$v_{in} \ll \frac{2}{(g_m/I_D)_1} \simeq 80mV \tag{B.3}$$

$$v_F \ll \frac{2\alpha}{(g_m/I_D)_{C1}} - \alpha n U_T = \alpha n U_T \simeq 4V \tag{B.4}$$

Proof

$$i_{out1} = \frac{1}{2} g_{m1} \left(\frac{g_{m8}}{g_{m5} + g_{m8}} + \frac{g_{m7}}{g_{m6} + g_{m7}}\right) v_{in} + \left(\frac{g_{m5} g_{m8}}{g_{m5} + g_{m8}} + \frac{g_{m6} g_{m7}}{g_{m7} + g_{m6}}\right) v_F \tag{A.12}$$

Assuming that $g_{m1} = g_{m7} = g_{m8} = \alpha g_{m9} = \alpha g_{m6} \equiv \alpha g_{mc}$ with $\alpha \gg 1$, and $I_{D1} = I_{D7} = I_{D8} = \alpha I_{D6} = \alpha I_{D9} \equiv \alpha I_{DC}$, and substituting in Eq. A.12 we have:

$$i_{out1} = g_{m1} v_{in} + 2 g_{mc} v_F \tag{B.5}$$

A way to analyze the multiplication effect is to see how the input signal perturbs the polarization (the dc current) of M5, M6, M7 and M8:

$$I'_{DC} = \frac{I_{D1} + \frac{1}{2} g_{m1} v_{in}}{\alpha} \tag{B.6}$$

The first condition directly arise from the previous equation:

$$I_{D1} \gg \frac{1}{2} g_{m1} v_{in} \Rightarrow v_{in} \ll \frac{2}{(g_m/I_D)_1} \tag{B.1}$$

Considering the general expression for g_m given by the ACM model [142] we have:

$$g_{mc} = \frac{1}{n U_T} \frac{2 I_{DC}}{1 + \sqrt{1 + I_{DC}/I_S}} \tag{B.7}$$

Then:

$$g'_{mc} = \frac{1}{\alpha n U_T} \frac{2(I_{D1} + \frac{1}{2} g_{m1} v_{in})}{1 + \sqrt{1 + \frac{I_{D1} + \frac{1}{2} g_{m1} v_{in}}{\alpha I_S}}} \tag{B.8}$$

Considering the first-order Taylor series of g'_{mc} we have:

$$g'_{mc} = g'_{mc}(0) + \frac{\partial g'_{mc}}{\partial v_{in}}(0) v_{in} = g_{mc} + \frac{\partial g'_{mc}}{\partial v_{in}}(0) v_{in} \tag{B.9}$$

$$\frac{\partial g'_{mc}}{\partial v_{in}}(0) = ... = \frac{\frac{1}{2} g m_1}{\alpha n U_T} \frac{1}{\sqrt{1 + \frac{I_{D1}}{\alpha I_S}}} \tag{B.10}$$

Substituting in Eq. B.5 leads to:

$$i_{out1} = g_{m1} v_{in} + 2 g_{mc} v_F + 2 \frac{\frac{1}{2} g m_1}{\alpha n U_T} \frac{1}{\sqrt{1 + \frac{I_{D1}}{\alpha I_S}}} v_{in} v_F \tag{B.11}$$

The second condition arise from impose that the first term in the right side is greater than the third term. If this is true, there won't be multiplication:

$$g_{m1} v_{in} \gg 2 \frac{\frac{1}{2} g m_1}{\alpha n U_T} \frac{1}{\sqrt{1 + \frac{I_{D1}}{\alpha I_S}}} v_{in} v_F \Rightarrow 1 \gg \frac{1}{\alpha n U_T} \frac{1}{\sqrt{1 + \frac{I_{D1}}{\alpha I_S}}} v_F \tag{B.12}$$

Then:

$$v_F \ll \alpha n U_T \sqrt{1 + \frac{I_{DC}}{I_S}} = \alpha n U_T \left(\frac{2 I_{DC}}{g_{mC} n U_T} - 1 \right) \tag{B.13}$$

Finally:

$$v_F \ll \frac{2\alpha}{(g_m / I_D)_C} - \alpha n U_T \tag{B.2}$$

Appendix C

Deduction of the thermal noise power spectral density

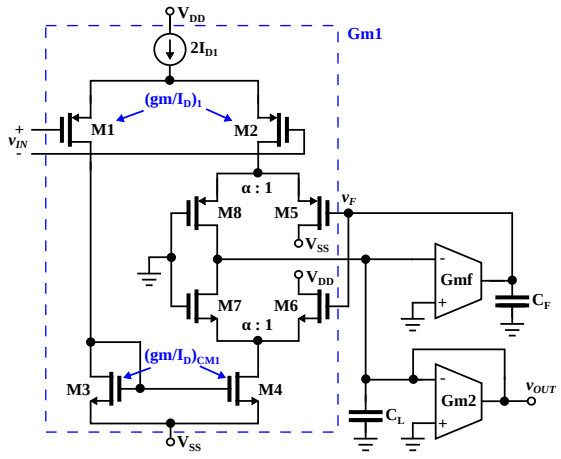


Figure C.1: Architecture.

Consider Fig. C.1. Only the noise contribution of Gm1 and Gm2 will be considered, because Gmf only have its input transistors connected to the output node of the circuit, thus its noise contribution is negligible.

Firstly, we will analyze the noise contribution of Gm1. The transistors of the current source $2I_{D1}$ introduce noise in common mode, thus they can be ignored. M5, M6, M7 and M8 are cascode transistor, for that reason the noise contribution of these transistor is negligible. Therefore, the main noise contributors are M1, M2, M3 and M4.

The input-referred noise power spectral density $S_{ni}^{M1,2}$ of M1 and M2 is simple to find, because these transistor are at the input:

$$S_{ni}^{M1} = S_{ni}^{M2} = \frac{\gamma_1 n_P kT}{g_{m1}} \tag{C.1}$$

where γ is the excess noise factor[1], n is the slope factor (the subscript indicates whether it is an NMOS or PMOS transistor), k is the Boltzmann constant and T is the absolute temperature.

If we consider that the current mirror M3-M4 perfectly copies ($g_{mCM1N} = g_{mM3} = g_{mM4}$), the noise contribution of M3 and M4 is the same. The noise current of these transistors directly flow to the output node v_{out}, and we have:

$$S_{ni}^{M3} = S_{ni}^{M4} = \frac{\gamma_{CM1N}.n_N kT g_{mCM1N}}{g_{m1}^2} \tag{C.2}$$

Combining Eq. C.1 and C.2 we have

$$S_{ni}^{Gm1} = \frac{2\gamma_{CM1N}.n_N kT}{g_{m1}} \left(\frac{\gamma_1 n_P}{\gamma_{CM1N} n_N} + \frac{(g_m/I_D)_{CM1N}}{(g_m/I_D)_1} \right) \tag{C.3}$$

According to Eq. C.3, M1 and M2 have to be biased in weak inversion (maximum (g_m/I_D)), and M3 and M4 in strong inversion (low (g_m/I_D)), thus we have:

$$S_{ni}^{Gm1} = \frac{2\gamma_{si} n_N kT}{g_{m1}} \left(\frac{\gamma_{wi} n_P}{\gamma_{si} n_N} + \frac{(g_m/I_D)_{CM1}}{(g_m/I_D)_1} \right) \tag{C.4}$$

where $\gamma_{wi} = 2$ and $\gamma_{si} = 8/3$ are respectively the excess noise factor in weak and strong inversion.

Secondly, we will analyze the noise contribution of Gm2 (see Fig. C.2). The transistors of the current source $2I_{D2}$ introduce noise in common mode, thus they can be ignored. M14 and M15 are cascode transistor, for that reason the noise contribution of these transistor is negligible.

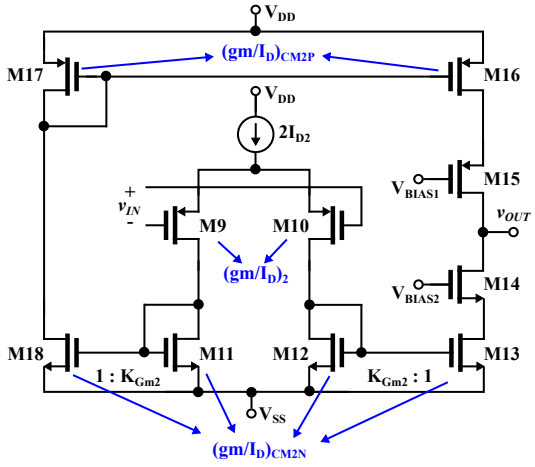


Figure C.2: Gm2 implementation at transistor level.

Therefore, considering the noise contribution of the input transistors (M9 and M10), the NMOS current mirror transistors (M11, M12, M13 and M18) and the PMOS current mirror transistors (M6 and M17) we have:

$$S_{ni}^{Gm2} \cong \frac{2\gamma_{si} n_N kT}{G_{m1}} \frac{I_{D2}}{I_{D1}} \Gamma \tag{C.5}$$

[1] γ_i corresponds to the input transistors of Gmi and γ_{CMij} to the current mirror transistors of Gmi, j indicates whether it is an NMOS or PMOS transistor)

where Γ is:

$$\Gamma = \frac{(g_m/I_D)_2}{(g_m/I_D)_1}\frac{n_N}{n_P K_{G_{m2}}^2} + \frac{(g_m/I_D)_{CM2N}}{(g_m/I_D)_1 K_{G_{m2}}^2} + \\ + \frac{(g_m/I_D)_{CM2N}}{(g_m/I_D)_1 K_{G_{m2}}} + \frac{(g_m/I_D)_{CM2P}}{(g_m/I_D)_1}\frac{n_N}{n_P K_{G_{m2}}} \quad (3.12)$$

Therefore, the total input-referred noise power spectral density S_{ni}^{total} is:

$$S_{ni}^{total} \cong \frac{2\gamma_{si} n_N kT}{G_{m1}}\left(\frac{\gamma_{wi} n_P}{\gamma_{si} n_N} + \frac{(g_m/I_D)_{CM1}}{(g_m/I_D)_1} + \frac{I_{D2}}{I_{D1}}\Gamma\right) \quad (3.11)$$

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Appendix D

High-ICMR implementation

This architecture essentially consist of replacing the Gm1 presented in Chapter 3 by the one depicted in Fig. D.1. This architecture enables a higher ICMR at the cost of increasing the power consumption (and therefore NEF). As mentioned in Chapter 3 this architecture was our starting point which was originally reported in [58].

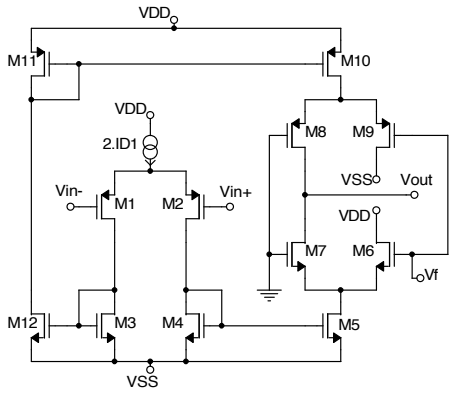

Figure D.1: High-ICMR preamplifier Gm1 implementation at transistor level.

Preliminary experimental results of two samples of the same chip, fabricated in a 0.5 μm standard CMOS process, are presented in Table D.1 and Table D.2 (part of them were reported in [141]).

Appendix D. High-ICMR implementation

Table D.1: Experimental results of two chips with external C_F = 22 nF.

	Simulation	IC#01	IC#02
Gain (dB)	46.4	46.7	47.0
$f_{high-pass}$ (Hz)	1.4	1.0	1.0
$f_{low-pass}$ (kHz)	7.7	7.7	7.5
Supply current (μA)	16.1	16.1	16.1
Input noise (μV_{rms})	3.1	N/A	N/A
NEF	5.5	N/A	N/A
CMRR (dB)	N/A	87.6	100.5
Gain w/$V_{IN,dc}$ = 50 mV (dB)	39.6	39.7	39.7
Gain w/$V_{IN,dc}$ = 100 mV (dB)	33.1	30.4	29.8
Output offset (mV)	1.0	15.1	14.3

Table D.2: Variation of CMRR with dc input $V_{IN,dc}$ with external C_F = 22 nF.

$V_{IN,dc}$ (mV)	CMRR @ 1 kHz (dB)
-100	93.6
-50	90.4
0	87.6
+50	85.1
+100	84.0

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