Ultra Low Power Pulse Generator Based on a Ring Oscillator with Direct Path Current Avoidance

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***Abstract*— This paper presents a wide frequency range, ultra low power pulse generator based on a ring oscillator. The proposed architecture avoids the direct path current, allowing to reach pulse frequencies down to the kHz range while maintaining the power consumption proportional to the frequency. Furthermore, the proposed topology for the current starved inverter circuit improves the symmetry between rising and falling edges of the output signals of the ring oscillator with respect to the traditional implementation. A frequency range from $1.75kHz$ to $10MHz$ consuming $1nW$ and $3.6\mu W$ respectively was achieved in a 130nm CMOS process. The modular design can be used to generate any non-overlapping pulse sequence with variable width.**

I. Introduction

Several mixed signal ultra low power circuits require simple generators of digital pulse sequences or patterns that control the operation of the analog part. This is the case of the application that motivates this work: switched capacitor DC/DC converters [1], where switches must be driven with sequential pulses and the frequency must be changed to achieve a good output voltage regulation. Voltage controlled ring oscillators (VCRO), usually based on "current starved" inverter circuits, are very useful circuits for the mentioned applications as well as clock generators or PLLs ([2], [3], [4], [5]). The aim of this paper is to present a novel voltage controlled digital pulse generator based on a VCRO. The improvements presented are applicable for pulse generator design but also to general VCRO design.

There are several papers about VCRO but all of them achieve wide frequency range variation without taking much care about power consumption. In [2] a $29.2mW$ power consumption is registered for a frequency of $407MHz$, and in [3] $35.05mW$ for a frequency of $368.9MHz$. In [4] an almost constant power consumption related to the frequency is registered which is a poor behavior for low power circuits where lower consumption is expected for lower activity.

CMOS inverters have three sources of power dissipation [6] which are static, dynamic (due to capacitance charge and discharge) and direct path (or short circuit current, SCC) power consumption. SCC depends on rise/fall times. As VCRO uses a variable rise/fall time for changing frequency, the lower the oscillation frequency is, the larger the power dissipated due to SCC for the conventional VCRO (shown in Fig. 1(a)). Therefore, to achieve low power consumption on lower frequencies, short circuit currents must be avoided. This paper presents an innovative architecture for the VCRO that avoids short circuit currents.

On the other hand, as mentioned in [3] and [4], traditional VCRO have a drawback, which is that for low frequency (small bias current) it is difficult to match falling and rising time. The proposed architecture for the VCRO improves this matching compare to the traditional one.

The paper is organised as follows. Section II presents the conventional architecture and the proposed architecture. After this, in Section III a comparison between the architectures in terms of power consumption and symmetry is done based on simulations. Finally, section IV presents the conclusions drawn from this paper.

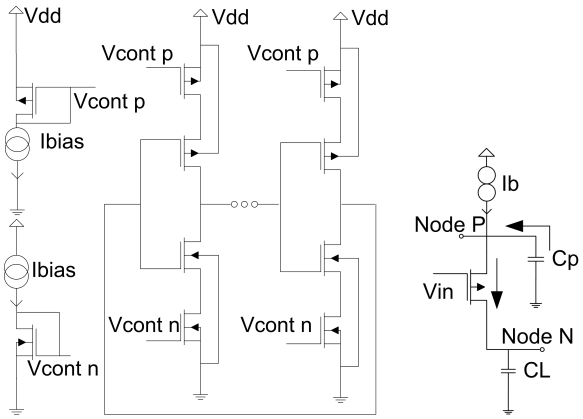
II. Proposed Architecture

An architecture capable of generating low frequency patterns using a VCRO is presented. As mentioned before, there are applications where a pulse sequence with a variable width and a low power consumption is needed. By means of the signals provided by the VCRO and through an XOR, a pulse sequence with variable width can be obtained (see subsection II-C). The main difficulty is to obtain a low frequency and ultra low power VCRO.

A. Conventional Architecture for VCRO

The conventional architecture for a VCRO is shown in Fig 1(a). This architecture has two major problems. When trying to achieve low frequencies, the power consumption due to SCC starts dominating over the dynamic power. Consequently, power consumption does not decreases proportionally to frequency. A solution to eliminate the SCC power consumption is presented, allowing to maintain the power consumption proportional to frequency at low frequencies.

The second major problem when trying to achieve low frequency is that in this architecture, the load current is not



(a) Architecture (b) Cause of asymmetry

Fig. 1. Conventional Architecture for current starved VCRO

limited by the current source during the whole process of charging the load capacitance. As shown in Fig. 1(b), there is an additional contribution of current provided by the parasite capacitance of node P. As this capacitance depends on the MOS transistor, there is a difference between rising edges and falling edges due to the differences between nMOS and pMOS capacitances. This problem is presented in Fig. 2, where the two charging stages can be differentiated: limited by the current source (Stage 2) and not limited by the current source (Stage 1). A solution for this problem could be to change the ratio between CL and Cp by increasing CL. The disadvantage of this method is that power consumption is increased. An architecture which improves the symmetry between rising and falling edges without jeopardizing power consumption is presented in the next subsection.

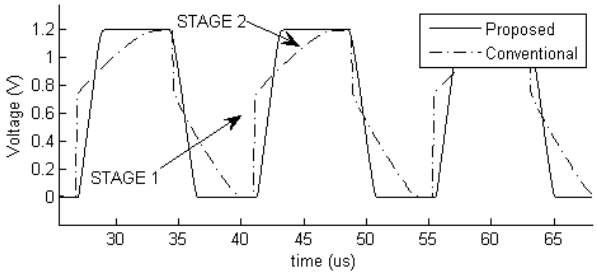
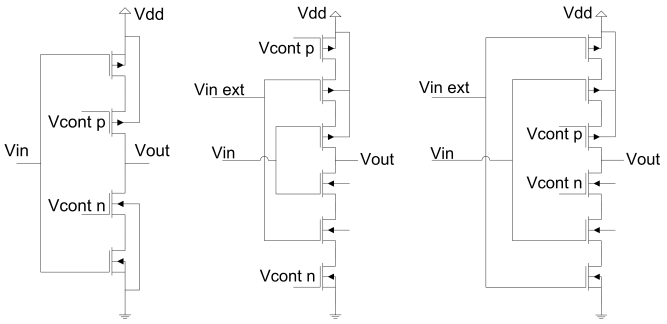


Fig. 2. Symmetry Problem

B. Proposed Architecture for VCRO

The proposed architecture is shown in Fig. 3(c). To improve the symmetry of rising and falling edges, the current source is placed in the center of the arrangement (Fig. 3(a) and 3(c)), assuring that the load current is limited by the current source during the whole charging process.



(a) Improvement on symmetry (b) Avoiding SCC (c) Improvement on symmetry and avoiding SCC

Fig. 3. Proposed Architecture

In order to eliminate the SCC, an external signal V_{inext} is used as shown in Fig. 3(b) and 3(c). The V_{inext} signal must change state before the V_{in} signal does. Consequently, it can be assured that at any time one transistor is completely cutoff so there is no direct path from V_{DD} to GND. This external signal is taken from a previous stage of the ring oscillator. Thus, the inverter works like a "break before make" switch, leaving its output floating during the delay between the switching in the external and internal signals.

C. Pulse Generator

As far as the pulse generator is concerned, a modular architecture is achieved, which can be used to generate a sequence of pulses with different widths. Fig. 4 shows the architecture proposed for the modular cell that implements each pulse output. This cell provides a clean pulse which starts when input signal A switches and ends before signal B switches.

In order to do this, the proposed cell has three different stages. The first one controls the pulse width, the second manages to regenerate the signal which is used to obtain the clean pulse. Finally, the third stage assures that signal B switches after the pulse finishes, compensating the XOR delay. Concatenating these modular cells and adding combinational logic, any pulse pattern can be generated.

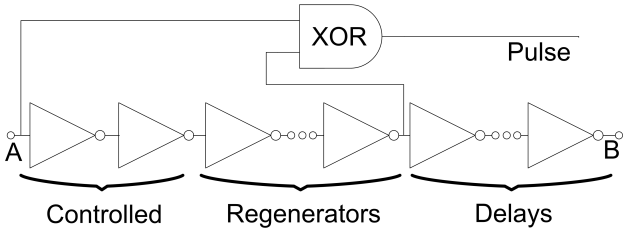


Fig. 4. Pulse Generator

The controlled stage consists of two inverters with a current source which limits the load current (Fig. 3(c)). As it was

explained before, this transistor is placed in the center of the arrangement in order to improve the symmetry. Regarding the SCC, it is important to observe that not every inverter is critical. Only the ones which have a slow input signal will have considerable SCC. The first controlled inverter of the cell and the ones from the delay stage have input signals which have been regenerated, and therefore it is not necessary to eliminate their SCC. On the other hand, the second controlled inverter and the regenerator stage are critical, hence the technique explained before is used to eliminate the SCC.

The signal used to eliminate the SCC (V_{inext} in Fig. 3(b) and 3(c)) is taken from the output of inverters of a previous cell of the ring oscillator. The delay from this previous cell to the cell where the signal is applied needs to be high enough in order to assure that the SCC has being eliminated, but not too high so that the output node does not float an unnecessary long time. Two signals from the last two regenerator inverters of each ring oscillator cell are applied as V_{inext} signals for inverters of following cells in the ring.

III. Simulation Results

In order to analyze the performance of the proposed architecture, four simulations were done concatenating four cells to generate four non-overlapping equal pulses. Each of this simulations tested a different architecture. The first one (**Conv**) used the conventional inverters (Fig. 1(a)) in the controlled stage. The second simulation (**Sym**) was made using the inverters shown in Fig. 3(a) in the controlled stage. Neither of them used the technique to avoid the SCC. In the third (**AvScc**) and fourth (**AvSccSym**) simulations the inverters used for the controlled stage were 3(b) and 3(c) respectively. In both of them the technique to avoid the SCC was implemented to the critical inverters.

TABLE I
INVERTERS PER STAGE

Stage	Number of inverters
Controlled	2
Regenerator	4
Delay	6

The number of inverters used in each stage were the same for the four simulations and are shown in Table I. The number of inverters in the controlled stage (for a given sizing) determines the frequency range that the pulse generator can achieve. The number of inverters in the regenerator stage determine the rise/fall time of the output pulse while the number of them in the delay stage determine the spacing between the pulses of two consecutive cells. The simulations were made in 130nm CMOS process using LP transistors.

TABLE II
TRANSISTORS SIZES

Transistors	nMOS (μm)	pMOS(μm)
Current Source	$W = 0.16$, $L = 2.4$	$W = 0.40$, $L = 2.4$
Delay inverters	$W = 0.16$, $L = 1.2$	$W = 0.40$, $L = 1.2$
Others	$W = 0.16$, $L = 0.12$	$W = 0.40$, $L = 0.12$

In Table II the size of the transistors used in the design are shown. There are three sizes: the transistor used for the current source, the transistors used for the inverters of the delay stage and the transistors used for the rest of the inverters including the ones used to avoid the SCC.

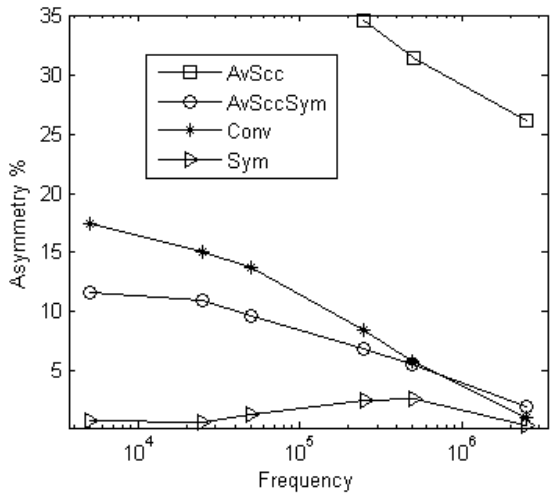


Fig. 5. Asymmetry

The difference between rising and falling edges of the ring oscillator pulses, shown in Fig. 2, leads to a difference of the pulse width of two consecutive pulses at the output of the XOR gate in Fig. 4. We will define the "asymmetry" of the pulse generator outputs as:

$$Asymmetry = 100\frac{(a-b)}{a} \quad (1)$$

Where a, b are the duration of each of the pulses with $a > b$. This is the meaningful definition for our application, where is intended that all pulses are equal. However, the asymmetry so defined is also a measure of the difference between rise and falling times of the ring oscillator outputs and the difference of the ring oscillator output duty cycle from 50%. The asymmetry is shown in Fig. 5 for each architecture as a function of the frequency.

Either using the technique to avoid the SCC or not, the symmetry is improved by changing the current source to the center of the arrangement. While the conventional architecture (**Conv**) has a poor symmetry within low frequency, the proposed one (**Sym**) has an almost constant

TABLE III
COMPARISON

Reference	[2]	[3]	[4]	[5]	this work
Supply voltage	5 V	3.3 V	3 V	1.8V	1.2 V
Technology (CMOS)	$0.8\mu m$	$0.18\mu m$	$0.6\mu m$	$0.04\mu m$	$0.13\mu m$
Frequency range	13Hz-407MHz	40Hz-380MHz	40Hz-366MHz	constant (10MHz)	1.75KHz-10MHz
Power Consumption	29.2mW@407MHz	35.05mW@368.9MHz	approx. 70μW@1MHz		284nW@1MHz
			approx. 70μW@10MHz	3μW@10MHz	3.6μW@10MHz
Rise time (10-90%)	N/A	.186ns@16Mhz	4.3ns@6MHz	N/A	1ns constant

asymmetry of less than 5%. Avoiding the SCC (**AvSccSym**) makes the symmetry worse but still better than the case of the conventional architecture.

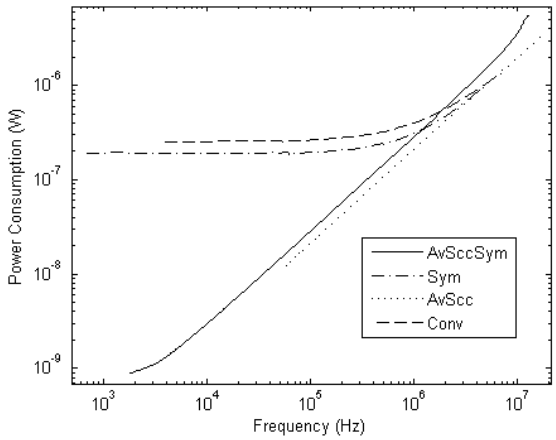


Fig. 6. Ring oscillator power consumption

Fig. 6 shows the ring oscillator power consumption for the four different architectures as the ring oscillator frequency was changed. It proves that avoiding the SCC, a wide frequency range can be obtained maintaining a linear consumption. The proposed architecture (**AvSccSym**) reaches a consumption more than two orders less than the conventional architecture for low frequencies. Certainly, when frequency rises, the benefits of avoiding the SCC decrease because the dynamic power consumption dominates.

As can be seen on Fig. 6, the AvScc architecture stops working under 100KHz. At low frequencies, the effect shown on Fig. 2 reduces the controlled inverter output swing. Moving the current source to the center of the arrangement improves the symmetry and also enables to reach lower frequency.

Even though this paper presents a pulse generator, the presented ideas can be applied in a clock generator using the output of a cell as clock output. This signal was regenerated, so it has a constant rise time of 1ns at any ring frequency. Further this signal has a duty cycle very close to 50% due to the improvement of symmetry in our circuit. In table III comparisons with the state of the art are presented.

IV. CONCLUSION

A pulse generator based on a current starved, voltage controlled ring oscillator has been presented. The proposed circuit improves the pulse and ring oscillator signals symmetry and reduces power consumption, particularly at low frequencies by avoiding direct path currents. The circuit can be also applied as a programmable clock generator. The designed circuit achieves a frequency range from $1.75KHz$ to $10MHz$ consuming $1nW$ and $3.6\mu W$ respectively. Since the signal is regenerated, a constant rise time of 1ns is obtained. The benefit of the proposed technique is assessed by comparing the results with the one of circuits designed in the same process with the conventional approach and with those that add separately each of the proposed features (symmetry improvement and direct path current avoidance).

Concatenating the proposed cells and adding combinational logic, any pattern could be generated changing the number of cells and inverters in the cells. In the tested arrangement, the width of the pulses varies between 10ns to 70us (8 pulses are generated by the 4 cells in each period of the ring oscillator), maintaining a energy consumption per pulse of less than 55fJ.

V. ACKNOWLEDGMENTS

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