A BIST Solution for the Functional Characterization of RF Systems Based on Envelope Response Analysis

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Abstract-- This paper presents a novel and low-cost methodology that can be used for testing RF blocks embedded in complex SoCs. It is based on the detection and spectral analysis of the two-tone response envelope of the block under test. The main non-linearity specifications of the block under test can be easily extracted from the envelope signal. The analytical basis of the proposed methodology is demonstrated, and a proposal for its implementation as a built-in test core is discussed. Finally, practical simulation examples show the feasibility of the approach.

I. INTRODUCTION

Nowadays, the advance in RF CMOS technologies has enabled the integration of complete transceivers in a single chip, which provides a significant reduction in manufacturing cost. However, there is a simultaneous increase in the cost of testing and diagnosis of these devices. Their diverse specifications and high operating frequency, as well as the large impact of process variations in current deep sub-micron technologies, make necessary extensive tests that are complex and expensive to perform. Reducing RF test complexity and cost is still an open research topic that has been addressed in a number of different approaches. Recent work in this area includes defect modeling and failure diagnosis [1]-[4], alternate test [4]-[5], DfT and BIST techniques [6]-[12], etc.

In particular, BIST techniques have been identified as a solution to mitigate RF test drawbacks for several reasons [9]:

a. The test cost of RF systems is dominated by expensive automatic test equipment (ATE). Thence it should be desirable to move some of the testing functions to the test board or to the device under test (DUT) itself.
b. There is a strong demand of known-good-die test solutions that can be implemented at wafer level, due mainly to the increasing packaging costs.
c. BIST can be used to identify faulty blocks inside the system, providing a valuable information for yield enhancement and accelerating product development.

On the other hand, an efficient BIST technique must meet the requirements of robustness, low area overhead, low design effort, available programming capabilities to accommodate the test program to the target measurements, and low-speed interface needs with the external ATE. Furthermore, BIST schemes (specially for complex Systems on Chip) must take advantage of on-chip resources that admit reuse, thus reducing the number of required additional components.

This work describes a new technique that can be used to improve the testability of RF blocks embedded in integrated transceivers, and that looks very suitable for a BIST implementation. It is based on the detection and analysis of the two-tone response envelope of an RF block. The envelope response signal is extracted using a simple diode-based envelope detector that can be easily implemented either on-chip or on an external test board. In both cases, the need of RF test equipment is eliminated since the response envelope is a low frequency signal compared to the operating frequency of the tested device. As it will be demonstrated, the main specifications of the block under test can be extracted from the envelope signal.

This presentation is organized as follows. Section II describes previous relevant work on RF test. Then, Section III presents the proposed approach, and discusses its mathematical basis from an analytical point of view. Section IV explicits an efficient BIST implementation of the proposed test technique. After that, Section V presents some simulation examples to validate the proposal. Finally, Section VI summarizes the main contributions of the new method.

II. PREVIOUS WORK ON RF TEST

Direct approaches for testing and diagnosis an RF device are based on the application of a high-frequency stimulus to the DUT and the observation of its response. This requires the use of high-speed external test equipment and, for embedded RF devices, the provision of an adequate test access. However, the increase in operation frequency and integration capabilities turns the latter two requirements quite difficult. Test access to internal nodes is usually impossible, and even in the case these nodes are reachable, there may be electrical losses in the transport of the signals from the chip to the external tester due to their inherent high-frequency.

Some papers [5],[13] replicate traditional RF test equipment such as spectrum analyzers on a load board. These approaches employ complex circuitry (mixers, frequency synthesizer, etc.) for up- and down-conversion of the test stimulus and its response, respectively. The need of RF testers is eliminated and multiple RF test specifications can be extracted. However, the load board circuitry is too complex for its direct BIST implementation, and hence this approach is limited to the test of discrete RF circuits.

The approach in [1]-[2] focuses on failure diagnosis of RF circuits. The work in [1] considers the detection of catastrophic faults, while that in [2] also attempts to isolate parametric ones. Although behavioral simulations demonstrate a high fault coverage, they lack a general fault model, and it is necessary the use of standard RF test equipment and techniques to enable failure diagnosis.

Loop-back test and diagnosis of transceivers have also been widely explored [3]-[4],[9]-[10]. The main advantage is that only-digital signals are involved as well as that both the receiver and the transmitter are tested at once. However, an on-chip implementation is not so simple since, in practice, some components need to be removed for testing, namely the band-pass filter, close to the antenna, and the power amplifier in the transmission path [20].

The use of test sensors embedded into the RF system has also been proposed [6]-[12]. Several built-in test schemes have been reported that use integrated peak, root-mean-square (RMS), and power detectors for testing discrete RF modules or complete transceivers. However, these sensors deliver a DC signal. To extract the test specifications from the limited information of a DC magnitude, multiple detectors and/or test configurations have to be used, thus increasing the complexity of the test as well as the required area overhead. Likewise, the design of these detectors is not always straightforward.

In this context, the work in [14] proposes the use of a very simple envelope detector for RF test purposes. This reference demonstrates that selected specifications can be extracted from the envelope of the response of an RF block to an optimized test stimulus. This response envelope can be acquired with a standard A/D converter and processed to carry out the demanded measurements. Nevertheless, the proposed method relies in a complex optimization algorithm to find the optimum test stimulus, complemented with the use of a multivariate-adaptive regression splines mapping for extracting the target specifications from the digitized envelope response.

The proposal to be described herein aims to extend the idea of testing by an envelope response characterization, but unlike [14], ours is directly based on analytical results, so there is no need of complex

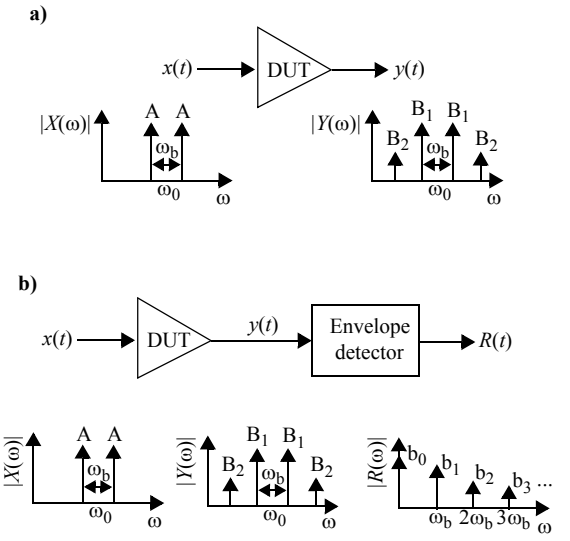

Fig. 1: a) Traditional two-tone test
b) Two-tone response envelope detection

stimulus optimization and regression models. Then, the pre-processing stage is eliminated. Furthermore, it will be demonstrated that processing the envelope can be greatly simplified, avoiding the need of a complete A/D converter for signal acquisition.

III. PROPOSED APPROACH

Fig.1a shows a standard two-tone test set-up that is traditionally used to characterize RF systems. In this test scheme, two high-frequency close tones are used as test stimuli and fed to the DUT. The system response is then acquired and conveniently processed to characterize the DUT. Important performance parameters such as forward gain, third-order intercept, inter-modulation products, 1dB compression point, etc, can be measured using this traditional set-up. However, the direct acquisition and processing of the test response is a challenging task, since this response is a high-frequency signal, that has to be handled by expensive RF test equipment.

Our approach, represented in Fig.1b, is in fact similar to the traditional scheme, but in this case the DUT response is driving an envelope detector. The extracted envelope has relevant information about the test response at much lower frequencies, this information being easily extracted by simplified processing. In what follows we will explain how the DUT response information is encoded in its envelope.

Let us consider the typical two-tone test (see Fig.1a), in which a non-linear RF device is driven by a signal $x(t)$ composed of two equal-magnitude tones at different, but very close, frequencies, in the form,

$$x(t) = A\cos\left(\left(\omega_0 - \frac{\omega_b}{2}\right)t\right) + A\cos\left(\left(\omega_0 + \frac{\omega_b}{2}\right)t\right) \qquad (1)$$

where A is the amplitude of each test tone, and ω_b is the frequency difference between them. Assuming, as it is the case in most situations, a third-order non-linear model for the RF block, the response $y(t)$ of the system can be written as,

$$y(t) = \alpha_1 x(t) + \alpha_3 x^3(t) \tag{2}$$

Expanding (2), and discarding the out-of-band components, the response $y(t)$ can be expressed as,

$$\begin{aligned} y(t) \cong & B_1 \cos\left(\left(\omega_0 - \frac{\omega_b}{2}\right)t\right) + B_1 \cos\left(\left(\omega_0 + \frac{\omega_b}{2}\right)t\right) + \\ & B_2 \cos\left(\left(\omega_0 - \frac{3\omega_b}{2}\right)t\right) + B_2 \cos\left(\left(\omega_0 + \frac{3\omega_b}{2}\right)t\right) \end{aligned} \tag{3}$$

The characterization of signal $y(t)$ in terms of the ratio B_2/B_1 is a measurement of the non-linear behavior of the system, and allows us to determine most performance figures such as IM3, IIP3, 1-dB compression, etc. However, the direct analysis of signal $y(t)$ is a challenging task when it comes from a RF transceiver, for instance. As discussed above, signal $y(t)$ may not be externally accessible, and even if it was, it would be necessary to use expensive high-frequency equipment to capture and process it.

Instead, we propose the analysis of the response envelope taking advantage of its frequency properties. Then, let $R(t)$ be the envelope of the response signal $y(t)$. Using the Rice formulation [15], $R(t)$ can be derived as

$$R(t) = \left| 2B_1 \cos\frac{\omega_b t}{2} + 2B_2 \cos\frac{3\omega_b t}{2} \right| \tag{4}$$

Signal $R(t)$ results to be a periodic function with period $T_b = 2\pi/\omega_b$, and hence, can be expanded in its Fourier series as

$$R(t) = b_0 + \sum_{k>0} a_k \sin k\omega_b t + b_k \cos k\omega_b t \tag{5}$$

where coefficients b_0, a_k, and b_k are given, respectively, by,

$$\begin{aligned} b_0 &= \frac{4}{\pi}\left(B_1 - \frac{B_2}{3}\right) \\ a_k &= 0 \\ b_k &= \frac{8}{\pi}\left(\frac{B_1(-1)^{k+1}}{4k^2-1} + \frac{3B_2(-1)^k}{4k^2-9}\right) \end{aligned} \tag{6}$$

Equation (6) shows that every harmonic component of $R(t)$ is a linear combination of the magnitudes B_1 and B_2, and hence, the ratio B_2/B_1 can be ideally derived from the frequency components of $R(t)$. In other words, the spectral analysis of the two-tone response envelope can be used to characterize the non-linear characteristics of an RF system.

IV. PRACTICAL BIST IMPLEMENTATION

The proposed test scheme requires the generation of a two-tone RF test stimulus, and the detection and spectral analysis of the DUT response envelope. While envelope detectors can be easily implemented on silicon, signal generation and spectral analysis are usually challenging and resource-consuming tasks when they have to be moved on chip.

This section proposes efficient methodologies for the spectral analysis of the response envelope and the generation of a two-tone test stimulus, suitable for an on-chip implementation.

A. Efficient on-chip spectral analysis of a two-tone response envelope

Traditional approaches for spectral analysis rely on an analog-to-digital conversion of the DUT outcome followed by the processing of the digitized signal by conventional algorithms (DFT, FFT, etc). This approach requires a full A/D converter and a complex DSP. Instead of that, since the response envelope is a low-frequency periodic function, its characterization can be made using an alternative method; in our proposal, by means of the efficient test core for periodic analog signal analysis depicted in Fig.2 (see [16]).

The functionality of this test core can be described as follows. The envelope signal under evaluation, $R(t)$, is modulated by two square waves in quadrature, $SQ_k(t)$ and $SQ_k(t\text{-}T_b/4k)$, of amplitude 1 and period T_b/k, where T_b is the period of $R(t)$ and k is an integer. The resulting signals $z_{1k}(t)$ and $z_{2k}(t)$ are fed to two matched 1st-order $\Sigma\Delta$ modulators, with an oversampling ratio, N, defined as $N=T_b/T_s$ (T_s is the sampling period in the $\Sigma\Delta$ modulators). The generated bit-streams d_{1k} and d_{2k} are integrated, along an integer number M of periods of the signal under evaluation, using a set of counters to obtain the parameters I_{1k} and I_{2k}. From them, a signature can be derived, Λ_k, defined as,

$$\Lambda_k = \sqrt{I_{1k}^2 + I_{2k}^2} \tag{7}$$

which can be proven to be related to the spectral components of signal $R(t)$,

$$\Lambda_k = \sqrt{I_{1k}^2 + I_{2k}^2} = \frac{MN2}{\pi}\left(|b_k| + \frac{1}{3}|b_{3k}| + \frac{1}{5}|b_{5k}| + \ldots\right) \pm 2 \tag{8}$$

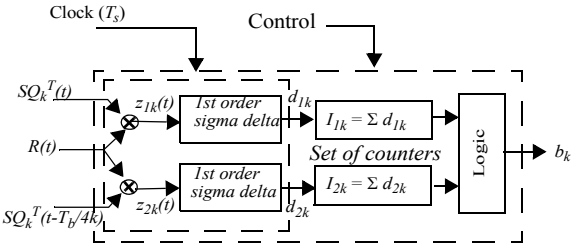

Fig. 2: Test core for the characterization of periodic signals

where magnitudes b_k are normalized with respect to the full-scale of the ΣΔ modulators, and M and N are, respectively, number of integration periods and the oversampling ratio, as defined above. It is worth to remark that these latter values determine the accuracy of our approach, the bigger they are, the more precise our method is.

Equation (8) can be approximated by,

$$\Lambda_k \cong \frac{2MN}{\pi} \cdot \frac{8}{\pi}\left|\frac{B_1}{4k^2-1} - \frac{3B_2}{4k^2-9}\right| \pm 2 \qquad (9)$$

Then, the computation of the first two signatures Λ_1 and Λ_2 (the most significative ones) allows us to the characterize the ratio B_2/B_1. Then, combining square-wave and first-order sigma-delta modulation, together with very simple digital operations, we are able to extract the magnitude of every harmonic component of $R(t)$ without the need of a full A/D converter and complex FFT algorithms.

B. Generation of a two-tone RF test stimulus

Usual approaches for the generation of RF test stimuli generate a low-frequency version of the desired signal and then perform an up-conversion using a mixer, which is a building block commonly available in many RF integrated systems, and hence may be adapted for its reuse during the test.

In this way, the generation of a two-tone RF stimulus composed of two equal-magnitude tones at different, but very close, frequencies, such as (1), can be realized by generating a low-frequency single tone at frequency $\omega_b/2$ and mixing it with a carrier at frequency ω_0, as it is depicted in Fig.3. The single-tone signal can be efficiently generated on-chip reusing existing resources in the RF system, namely an integrated DSP and a DAC, if they are available, or using simpler signal generation techniques for BIST [17]-[18] that only require a low-frequency clock to provide the desired tone. The high-frequency carrier can be provided by a frequency synthesizer (in the case this is already present in the RF system under test), or externally provided.

However, in any case, the proposed spectral analysis methodology requires the oversampling ratio $N=T_b/T_s=\omega_s/\omega_b$ to be an integer number. That is, the ratio between the sampling frequency in the ΣΔ modulators forming part of the analyzer block, ω_s, and the frequency of the response envelope, ω_b, has to be accurately controlled. This requirement can be easily fulfilled using the clocking scheme in Fig.3. Its functionality can be described as follows. A master clock at frequency ω_0 is used to clock directly the up-conversion mixer, while a $1/k$ division of this master clock is used for the evaluation block. Given that the single-tone generator provides a signal at $1/n$ the frequency of its clock, then clocking the generator at a $1/(2N/n)$ division of the evaluator clock frequency achieves the desired ratio $\omega_s/\omega_b=N$ by construction. In this way, choosing the values of N and n conveniently, the desired synchronization can be achieved using only simple integer divisions of a master clock.

V. APPLICATION EXAMPLE

The proposed characterization approach has been validated by behavioral simulations in Verilog-A. The objective of these simulations is the characterization of the non-linear behavior of a typical RF block in terms of the ratio B_2/B_1. For this example a Low Noise Amplifier (LNA) has been used as DUT. The LNA under test is driven by a two-tone at-speed stimulus, and its response envelope is extracted and processed as explained in the previous section.

A realistic model of the LNA have been realized according to the guidelines in [19]. Its performance figures, which are listed in Table I, correspond to typical specifications of commercial LNAs.

The envelope detector in this simulation has been modeled by a typical diode-based detector shown in Fig.4, in which the diode has a piece-wise-linear

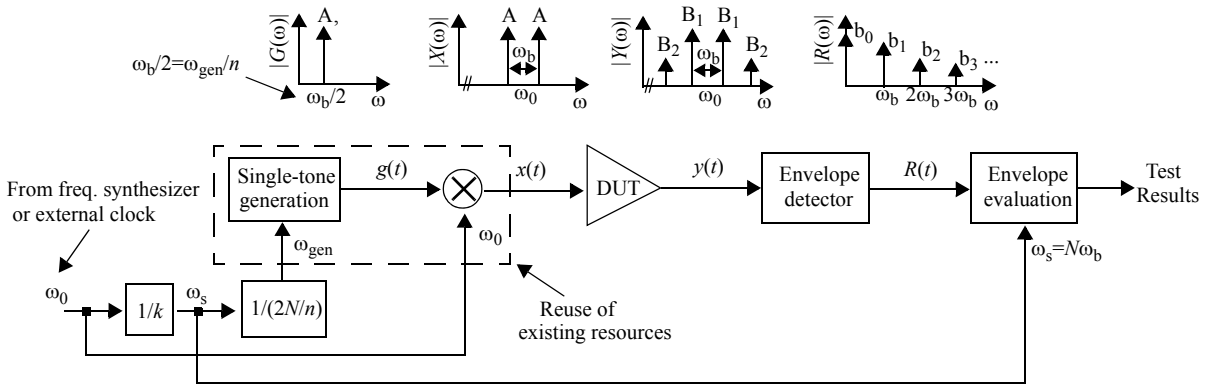

Fig. 3: Proposal for a full-BIST implementation

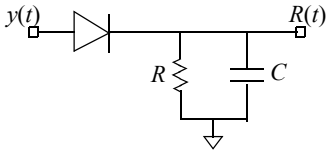

Fig. 4: Envelope detector model

characteristic, and the *RC* constant of the detector has been properly selected to follow the envelope coarsely. It is important to notice that there is no need of an accurate envelope detector, since accuracy is much more dependent of parameters *M* and *N*. The ripple voltage introduces high frequency components that will be attenuated by the proposed spectral analysis method. In any case, a superdiode circuit can be implemented, still with a low cost, by adding an operational amplifier. Doing this, impedance adaptation can be optimized without penalties. The simulation parameters used for the LNA and the modulators are listed in Table I. Fig.5 shows the waveform of the obtained response envelope. Notice that the ripple voltage is in the range of an 8% of the response envelope peak value.

LNA specifications	Gain	16dB
	OIP3	34dBm
	NF	1dB
ΣΔ modulators	*N*	96
	FS	1.2V
Test stimulus	*A*	100mV
	f_0	1GHz
	f_b	1MHz

Table I:Simulation parameters

Signatures Λ_1 and Λ_2 of the response envelope have been extracted, and the ratio B_2/B_1 was computed. The simulation results are listed in Table II for different number of evaluation periods, *M*. As it was expected, this Table shows that the measured ratio approaches the theoretical value as the number of evaluation periods increases.

Number of evaluation periods, *M*	Measured B_2/B_1	Actual B_2/B_1
1	< –17 dB	–56 dB
2	< –24 dB	
5	< –36 dB	
10	< –42 dB	
20	< –44 dB	
100	[–53 dB, –48 dB]	

Table II:Measurements of the B_2/B_1 ratio as a function of the number of evaluation periods, *M*

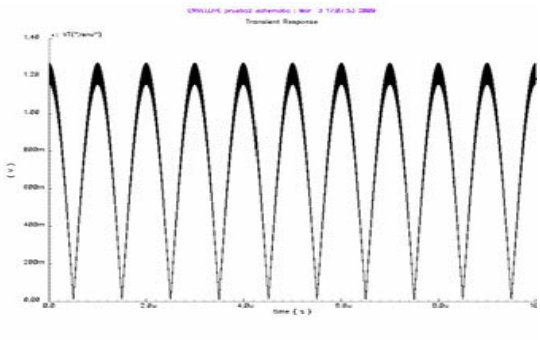

Fig. 5: Obtained response envelope

VI. CONCLUSIONS

A novel methodology for the characterization of the non-linear characteristic of embedded RF systems have been presented. It is based on the analysis of the envelope of the system response to a two-tone at-speed stimulus.

From a hardware point of view, the proposed test core is reduced to a simple low-performance envelope detector, together with two first-order ΣΔ modulators, while the generation of the test stimulus can be easily performed reusing on-chip resources. Advantages of the proposed approach are that there is no need of high-frequency signal processing nor of a full A/D converter. This makes the proposed test core simple to implement and very suitable for its inclusion in an on-chip BIST scheme.

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