A 2.4GHz LNA in a 90-nm CMOS Technology Designed with ACM Model

Rafaella Fiorelli, Fernando Silveira
Instituto de Ingeniería Eléctrica
Universidad de la República
Montevideo,Uruguay
{fiorelli,silveira}@fing.edu.uy

Eduardo Peralías, Diego Vazquez,
Adoración Rueda, José Luís Huertas
Instituto de Microelectrónica de Sevilla,
CNM-CSIC
Universidad de Sevilla
Seville, Spain
{peralias, dgarcia, rueda,
huertas}@imse.cnm.es

ABSTRACT

As part of a Low-IF ZigBee receiver, a 2.4GHz di®erential common source low noise ampli¯er, implemented in a 90nm mixed/RF 7M CMOS process and designed in moderate inversion, is presented in this work. Design methodology and simulation results from Spectre-RF simulator are presented. With 2.5V supply voltage, the LNA achieves a noise ¯gure of 2.5dB, an IIP3 of 1dB and gain higher than 10dB, with a current consumption of 12mA. The LNA area without pads is 720¹*m* £ 710¹*m*.

Categories and Subject Descriptors

B.7 [Hardware]: Integrated Circuits

General Terms

Design, Algorithms, Theory

Keywords

radio-frequency, low noise ampli¯ers, ACM model, design methodology

1. INTRODUCTION

Nowadays, study and design of radio-frequency front end analog blocks in CMOS technology have had an important development due to the considerable reduction in the transistor's channel size. Technologies commercially available reach transistor lengths up to 45nm, making possible transistors with transit frequencies f_T much higher that the microwaves, even working in moderate or weak inversion [1]. Also there are important improvements in integrated passive components, i.e. inductors and capacitors, which have reached high levels of quality and low dispersion values. These two facts make the design in microwaves an accessible matter to radio-frequency designers.

The low noise ampli¯er is the ¯rst block of a receiver. Its most important function is to increase the input signal to overcome the noise generated in the following stages of the system. In this work the circuit implemented is a di®erential common source LNA (CS-LNA from now on) with source degeneration. These CS-LNAs have already been studied ([2], [3]) and several schemes were developed to reduce noise and/or current consumption [4]. In our case, the scope was put in minimizing the noise ¯gure (*NF*) without surpassing the current consumption of previous published conventional CS-LNAs with source degeneration ([5], [6], [7]) which reach values up to 10mA for single-ended devices. Also a design methodology has been developed using the one-equation all-region ACM model to explore the design space.

The CS-LNA presented is part of a ZigBee receiver working in the 2.4GHz band; it was designed and currently being fabricated in a 90nm CMOS technology. ZigBee standard imposes certain constraints which can be translated to electrical characteristics of the receiver (noise, gain, linearity, among others). The noise added to the input signal is studied using the *NF* characteristic, initially speci¯ed in less than 5dB. Linearity is studied through the third order intermodulation point IP3[1]; which must be higher than -5dB. The di®erential output impedance was set to 100- to match the input impedance of the following block, a di®erential mixer; for this reason we have chosen a di®erential LNA. The input impedance was set to 100- to facilitate measurements and coupling with an external antenna. In Table 1 the principal requirements of this CS-LNA are shown.

1.1 The ACM model

For the theoretical deductions and simulations, the one-equation- all-region MOSFET model in [8], [9] has been used to describe the transistor behaviour. This is a physical-based compact model valid for all inversion levels which conserves charge and preserves the symmetry of the transistor. In this design, the transistors are considered to be working in the saturation region. In the ACM model, the drain current is expressed as the di®erence between the forward I_F and

[1]If U is the amplitude of an input sinusoidal signal and IM3 is the third order intermodulation product then IP3 is the U value at which IM3 extrapolates to one

Design requirements	Value
Voltage	2:5V
Current	¼ 10mA
Frequency	2:4GHz ¡ 2:48GHz
Gain	¸ 10dB
Noise Figure	· 5dB
IIP3	¸ ¡5dBm
Input impedance	100-
Output impedance	100-

Table 1: Requirements of the ZigBee CS-LNA

reverse I_R components.

$$I_D = I_F(V_G;V_S) ¡ I_R(V_G;V_S) = I_S ¢ (i_f ¡ i_r) \quad (1)$$

$$I_S = \frac{1}{2} n ¹ C_{ox}^{o} Á_t^2 \frac{W}{L} \quad (2)$$

I_S is the speci¯c current, which is proportional to the aspect ratio of the transistor. V_G, V_S and V_D are the gate, source, and drain voltages, with reference to the substrate. Here, ¹ is the e®ective mobility, $Á_t$ is the thermal voltage, C_{ox}^{o} is the gate oxide capacitance per unit area and n is the slope factor [10], slightly greater than unity and weakly dependent on the gate voltage. Parameters i_f and i_r are the normalized forward and reverse currents, or inversion levels at source and drain, respectively. In the saturation region, drain current is almost independent of V_D; therefore, $i_f >> i_r$ and I_D »= I_F. The inversion level i_f (i_r) represents the normalized carrier charge density at the MOSFET source (drain) Q_{IS}^{o} (Q_{ID}^{o}). The small-signal transconductances g_m, g_{ms} and g_{md} (gate, source and drain transconductances) are given by

$$g_{ms(d)} = ¡ ¹ \frac{W}{L} Q_{IS(D)}^{o} \frac{2I_S}{Á_T} ¡ \sqrt{1 + i_{f(r)}} ¡ 1 ¢ \quad (3)$$

$$g_m = \frac{g_{ms} ¡ g_{md}}{n} \quad (4)$$

The other small-signal parameters can also be derived in terms of the inversion level. For the sake of simplicity a complete list of expressions is not here presented, but ACM intrinsic capacitances and transit frequency f_T equations [8] were employed throughout the design process.

2. LNA DESIGN

2.1 Circuit description

The circuit topology is shown in Fig. 1; it is a di®erential common source narrowband (CS-LNA) with inductive source degeneration. Considering the single-ended equivalent of this circuit, it can be divided in two stages. The ¯rst one provides the input impedance and the gain required, and is conformed by the transistor M_1, the gate inductance L_g and the source inductance L_s. The second stage comprises the transistor M_2, the drain inductance and resistance (L_d and R_d respectively), and the capacitors C_{d1} and C_{d2}. Transistors M_1 and M_2 form a cascode stage; so M_2 can be seen as a decoupler between the output impedance network and the input one. L_d, R_d and C_d are part of the output impedance network. In this design, M_2 size was chosen arbitrarily equal to M_1 size [3](in future work, M_2 size optimization should be considered in order to reach smaller noise

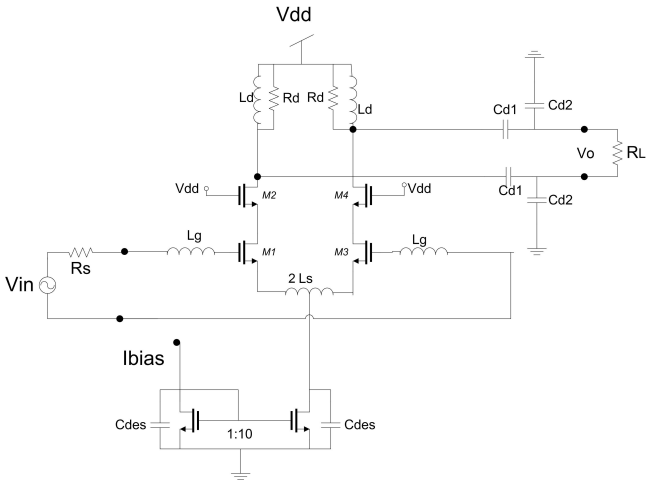

Figure 1: Di®erential CS-LNA designed. [7](Input biasing and matching not shown)

¯gure). Source degeneration topology is used as it gives a real input impedance for a frequency f_0 without any noise overhead, contrary to what happens in con¯gurations where a resistive component is added at the input, e.g. CS-LNA with shunt input resistor, shunt series LNAs or common gate LNAs ([2], [7]). Due to the topology characteristics it is a narrowband device, because the input impedance is real only at the resonant frequency $!_0$.

Input impedance is:

$$Z_{in}(s)|_{s=j!_0} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L_s \Big|_{s=j!_0} = \frac{g_m}{C_{gs}} L_s = !_T L_s \quad (5)$$

where

$$!_0 = \frac{1}{\sqrt{(L_g + L_s) C_{gs}}} \quad (6)$$

At f_0, the overall stage transconductance results to be almost independent of g_m, the M_1 transistor transconductance,

$$G_m(!)\Big|_{!=!_0} = \frac{i_{M1}}{v_{in}} = \frac{i_{M1}}{v_{gs1}} \frac{v_{gs1}}{v_{in}} = g_m ¢ Q_{in} \Big|_{if R_s = !_T L_s} = \frac{g_m}{!_0 C_{gs} (R_s + !_T L_s)} = \frac{1}{2!_0 L_s} \quad (7)$$

where $Z_{in}(!_0) = R_s = !_T L_s$ has been considered.

With an output load R_L=2 in each branch, the voltage gain is:

$$G(!_0) = \frac{v_{out}}{v_{in}} = G_m(!_0) ¢ \frac{R_L}{2} = \frac{!_T}{!_0} \frac{R_L}{4R_s} \quad (8)$$

From (8) for ¯xed values of f_0, R_s and R_L, a circuit gain increment is reached only by raising f_T.

2.2 Design methodology

The methodology proposed here starts for a single-ended CS-LNA. For a complete design, the following parameters must be computed: L_g, L_s, M_1 width W_{M1}, M_1 drain current I_{D1}. M_1 transistor length L_1 is chosen the smallest available, entitling to reach the highest f_T for a certain I_{D1}. Requirements of *NF*, *IIP3*, Z_{in} and gain must be ful¯lled; also restrictions of maximum current, and inductor values must be taken into account.

To study the LNA's characteristics, the small-signal circuit of Fig. 2 is considered ([11], [12]), where bonding inductance L_{bw}, pad capacitance C_p and an input matching network C_{M1}-L_{M1} (to adjust the LNA input impedance to R_s in case the requirement is not reached) are included. Considering the plane (I) of the circuit of Fig. 2, the impedance seen from the plane must be real as the admittance at this point should be cancelled at the working frequency. If R_p is less than R_s, an input matching network L_{M1}-C_{M1} is needed. The impedance seen at the left of the plane (II) is $Z_p = R_{eq} + j!_0 L_{eq}$ where R_{eq} and L_{eq} depend on R_p, C_p, L_{bw} and $!_0$. In this situation, the working frequency is

$$!_0 = \frac{1}{\sqrt{(L_{eq} + L_s)C_{gs}}} \tag{9}$$

and the input impedance must be:

$$R_{eq} \gg R_{in} = !_T L_s \tag{10}$$

NF is expressed as :

$$NF = 10log(F) \tag{11}$$

with *F*, the Noise Factor, given by [7] [13]:

$$F \gg 1 + \frac{\circ}{\circledR}\frac{\hat{A}}{Q_L}\frac{!_0}{!_T} \tag{12}$$

where ° is the channel thermal noise coe±cient and ® = $\frac{g_m}{g_{d0}}$ -following the notation of [7]-; Q_L is the quality factor of L_g and $\hat{A}$ is equal to:

$$\hat{A} = 1 \; ¡ \; 2jcj\sqrt{\frac{\pm\circledR^2}{5\circ}} + \frac{\pm\circledR^2}{5\circ}(1 + Q_L^2) \tag{13}$$

where *c* is the correlation coe±cient between M_1 gate and drain current noise (c ' ¡0:395j) and ± is the gate noise coe±cient.

An approximate value of *IIP3* is calculated using expressions cited in [3] and [11],

$$\begin{aligned} IIP3(dB) = \; & 11{:}25 + 10log(V_{GST}(2 + £V_{GST}) \\ & (1 + (£V_{GST})^2))) \\ & ¡10log(£) \end{aligned} \tag{14}$$

where $V_{GST} = V_{GS}¡V_T$, and £ is the mobility modulation coe±cient [11]. This expression is valid for strong inversion, so di®erences will appear when used in moderate inversion.

The gain value *G* is the starting point of the design °ow; from (8) we obtain the L_s value (considering R_L ¯xed). With L_s and R_p, $!_T$ is calculated from (10) and it is used to ¯nd i_f using the ACM model. To ¯nd W, we use the fact that for each i_f exists a relation between *NF* and the transistor width W. It is shown in Fig. 3 where *NF* is plotted versus *W=L* ratio for several i_f. For the inversion level found , W is chosen to meet a particular NF. If the values of

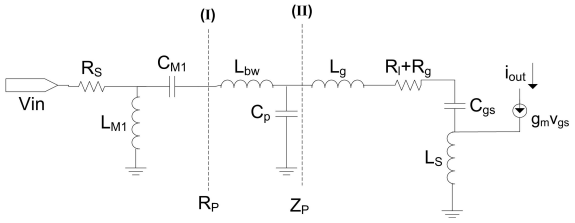

Figure 2: CS-LNA small signal model, with input adaptive network $C_{M1}¡L_{M1}$, bonding inductance L_{bw} and pad capacitance C_p included.

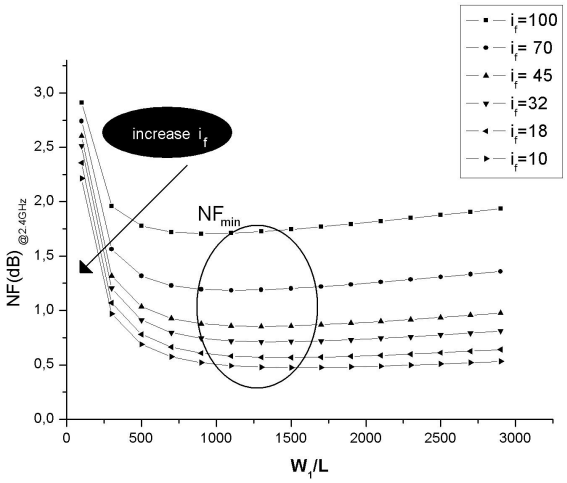

Figure 3: *NF* versus W/L ratio for various i_f values obtained with ACM model.

NF and *IIP3* -obtained from (11) and (14)- are acceptable, then C_{gs} is calculated using the ACM model. Finally from (9), L_g is obtained.

If the requirements of *NF* or *IIP3* are not satis¯ed, R_p could be changed, at the expense of the addition of an input adaptive network.

The design methodology is outlined in Fig. 4. A MATLAB program was implemented using the ACM model and the previous design equations.

In Fig. 3 a minimum *NF* (NF_{min}) is found for a certain W and for each i_f. Also we can see that when we move towards zones of stronger moderate inversion (M.I.), *NF* increases its value but not enough to be outside the requirement. Therefore a good trade o® between the values of *NF* and I_D can be reached working in moderate inversion and choosing the right W/L ratio. In this design, the CS-LNA was designed for the NF_{min} of the calculated i_f.

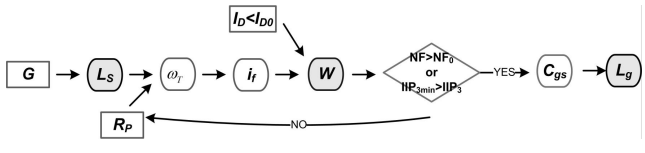

Figure 4: CS-LNA design methodology using ACM model

Component	Value
$W_{M1:::M4}$	28 £ (10=0:28)*um*
L_g	5.25nH
2 £ L_s	2 £ 330*pH*
L_d	3.2nH
R_d	75-
C_{d1}	7.6pF
C_{d2}	0.9pF

Table 2: Di®erential design components

Therefore, we obtained a CS-LNA design whose component values for the di®erential one are listed in Table 2.

It is important to point out that as our receiver is speci-ed to work with a 2.5V supply, according to the technology design rules, the minimum transistor channel length was limited to 280nm, despite the technology has a minimum channel length of 90nm. This important design constraint limits the optimization, particularly referring to voltage gain.

Impact of ESD protection. The design methodology does not include the ESD protection parasitics. In the design chosen, there is a low impact in its f_T and *F* parameters. In [14] it is shown how f_T and *F* are modi-ed by a factor of 1 + C_{ESD}=C_g, where C_{ESD} is the parasitic capacitance added by the ESD circuit. In this case this factor is around 1:2, which is not too high to spoil these LNA characteristics.

2.3 Inductors

The inductors are themselves a restriction in the design because of the limited range of values available in the technology. The L_g value is limited by the working frequency and the inversion level. From (9), L_g is calculated with $!_0$ and C_{gs}. L_g could be out of range specially for strong (weak) inversion, where C_{gs} would be very small (big)-. In our case, for i_f = 45 (M.I.), L_g = 5:25*nH*. Special arrangements with the manufacturer were made to control the bonding inductance value L_{bw}, around 1nH.

L_s is inversely proportional to the gain (see (8)), thus, for high gains, L_s would be out of the available range.

There is also a trade-o® between gain and input resistance. The gain expression at (8) considers that $!_T L_s = R_s$, and then G depends only L_s. However, if the L_s obtained is sufciently small and $!_T$ is not so high, it is possible that $!_T L_s$ does not reach R_s. Therefore, for this circuit, a matching network should be used. In our design the -nal value of L_s is 330pH. This value can be implemented because of the differential characteristic of the LNA, as there is no in°uence of the ground bonding inductance.

Both L_g and L_s are library inductors, implemented with stacked metal wires to reduce the series resistance.

2.4 Layout techniques

As this is a di®erential circuit, special attention was paid to make the layout as symmetric as possible. The optimum position of the -ve inductors is important as they occupy a considerable amount of area. The technology used provides di®erential inductors with under-nano Henry values and L_s was fabricated in that way.

The transistors were multi--ngered and double guarded. All the blocks were common-centroid designed. Decoupling capacitors between voltage supply and ground were added. Stacked metal ground tracks were inserted in the middle of the circuit to shield the blocks involved -inductors and transistors-. Process I/O RF and Mixed signal pads with ESD protection were used. In Fig. 5 -nal layout of the CS-LNA (without pads) is shown.

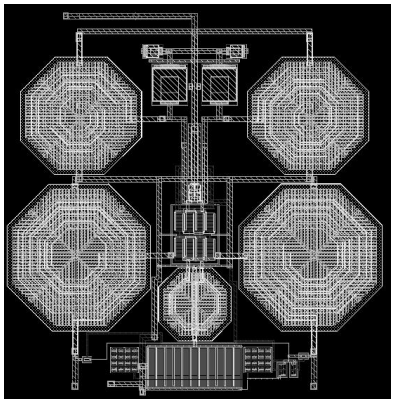

Figure 5: Final layout of the CS-LNA under fabrication.

Characteristics	Value @ 2.45GHz
Current consumption	12.5mA
S_{21}	11dB
S_{11}	-34dB
S_{22}	-29dB
$-S_{12}$	42dB
NF	2.5dB
IIP3	1.0dBm

Table 3: Spectre-RF simulated characteristics of the designed CS-LNA

3. SIMULATION RESULTS

After having designed the CS-LNA using ACM equations in MATLAB, typical and corner simulations were done using BSIM4 transistor model in the Spectre-RF simulator. Library inductor manufacturer's models were used.

All Spectre-RF simulations were done including the designed input network, the I/O ring cells and the package model. Simulations with the extracted circuit considering the parasitics were also performed to check the results.

In Table 3 the typical simulated characteristics are shown. It should be pointed out that the gain, *NF* and *IIP3* values are better than the initially proposed limits. However, current consumption is higher than expected, so the trade-o® between current consumption and *NF* should be considered in future work. Despite not shown, it should be also mentioned that all corner simulations performed comply with the initial requirements.

Behaviour of S_{11}, S_{12}, S_{21}, S_{22} and *NF* at frequencies around 2.4GHz are shown in -gures 6 to 10. At the band of interest (2:40*GHz* ¡ 2:48*GHz*) S_{21} is maintained above 10dB and S_{22} is below -15dB, the reverse isolation is higher than 40dB -a good value according to [3]. The *NF* has a di®erence of around 1dB respect of the MATLAB results, which is due to bias and M_2 transistor noise. Simulated IIP_3 is plotted in Fig.11.

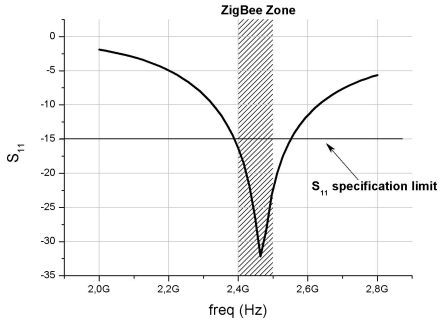

Figure 6: S_{11} parameter.

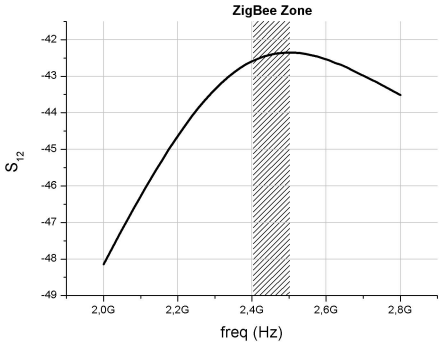

Figure 7: S_{12} parameter.

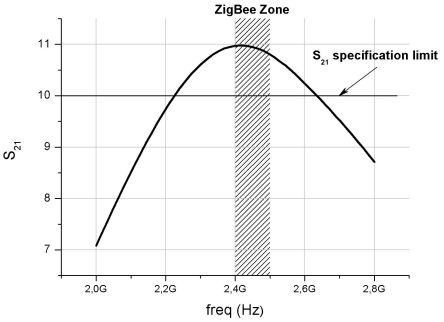

Figure 8: S_{21} parameter.

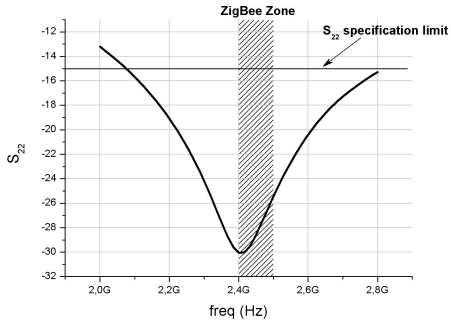

Figure 9: S_{22} parameter.

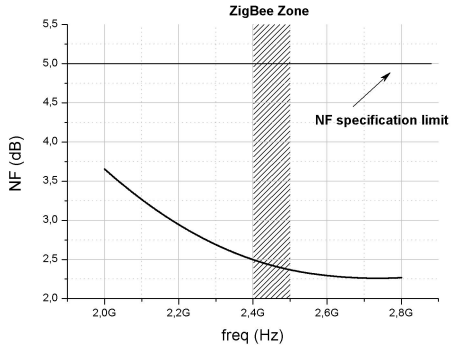

Figure 10: *NF* simulation of the di®erential circuit including bias and package

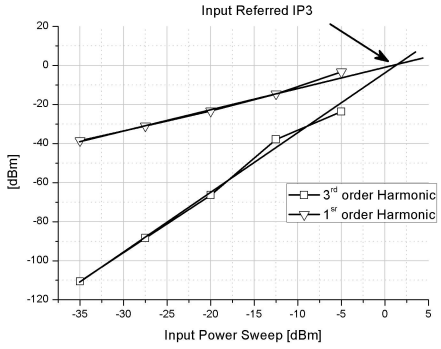

Figure 11: *IIP3* of the di®erential circuit

4. CONCLUSIONS

A 2.4GHz ZigBee di®erential CS-LNA was designed in a 90nm CMOS technology using the ACM model and working in the limits of moderate inversion. All the requirements were ful¯lled, except for the input impedance, thus a matching network was designed. The receiver, which includes this design, is currently under fabrication.

5. ACKNOWLEDGMENTS

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